Injection Locking Techniques for CMOS-Based mm-Wave Frequency Synthesis

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Dear reader,

with gladness I present you my Ph.D. thesis. It deals with Injection Locking Techniques for CMOS-Based mm-Wave Frequency Synthesis. Thanks to injection locking, high frequencies such as millimeter waves can be handled on a standard digital CMOS technology. The fascinating challenge of injection locking resides in the fact that we want to synchronize, with an external reference signal, the oscillatory response of an unstable system such as an oscillator. This duality between synchronization and oscillatory response has been inspiring me along the whole Ph.D. research. I think I can say that this duality has been translated into another one, typical of so many Ph.D. students: giving structure to a passionate research.
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As Ph.D. student and as young man, I feel grateful to so many people, who have accompanied me during this journey towards the Ph.D. degree.

I am now writing on board of a ship, sailing from Salerno to Messina. I see the many people, whom I acknowledge, as members of a crew: each one with a particular contribution to the journey of my Ph.D. research. Sometimes the sea was sweet and calm. Sometimes it was stormy and scaring. Well, this crew has never left me alone, even though I may have not always realized it.

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After all, Ph.D stays for Doctor of Philosophy!

Giovanni Mangraviti,
on the sea route from Salerno to Messina,5 January 2015
Abstract

Mm-wave frequencies offer opportunities for many wireless applications like high-data rate wireless communication (e.g. 60 GHz data links with datarates higher than 1 Gbit/s), automotive radars (e.g. 79 GHz car radars) and image sensors (e.g. 94 GHz). Modern CMOS enables the realization of mm-wave transceivers thanks to its speed increase and (relative) low cost.

One of the main challenges in mm-wave CMOS transceivers is the synthesis of the local oscillator (LO) signal. Traditionally, phase-locked loops (PLLs) are used for this task. Mm-wave PLLs require mm-wave frequency dividers. Traditionally, static current-mode logic (CML) latches are used as frequency dividers, but they require large power consumption at mm-wave. For this reason, alternative approaches are needed, such as low-power inductor-less mm-wave injection-locked frequency dividers (ILFDs) and LO synthesis based on subharmonic injection locking techniques.

Inductorless mm-wave ILFDs can work at high frequency, consume a small amount of power, can be tuned over a wide frequency range and are compact. The drawback is that they are sensitive to supply disturbances. This Ph.D. has devised an inductorless injection-locked 60-15 GHz ILFD, with a low supply sensitivity, in 40 nm CMOS.

A mm-wave LO frequency synthesizer, for instance at 60 GHz, based on subharmonic injection locking consists of three main parts: a lower-frequency PLL running at a subharmonic frequency $60/n$ GHz (with $n$ integer, odd for differential circuits), a $60/n$ GHz LO distribution and a 60 GHz subharmonically injection-locked oscillator (SHILO). Apart from the absence of 60 GHz dividers, another advantage is that the phase noise of the 60 GHz SHILO is shaped and thus lowered by the injected $60/n$ GHz signal.

This Ph.D. has investigated and proven the application of subharmonic injection locking technique for 60 GHz LO generation. First, a 60 GHz LO system has been designed in 90 nm CMOS. Here, the main challenges for a robust LO operation have been recognized: the narrow locking range of the 60 GHz subharmonically injection-locked QVCO (SHIL-QVCO) and the need for lock detection. Secondly, a novel 60 GHz SHIL-QVCO has been devised and realized in 40 nm CMOS. The use of coupled-LC tanks allows for a large locking range (more than 8 GHz, tunable over 52-66 GHz), thus enhancing the robustness of the system. At last, an improved 60 GHz SHIL-QVCO with calibration circuitry and lock detection has been realized in 40 nm CMOS. The SHIL-QVCO uses
coupled-LC tanks, achieving more than 2 GHz locking range tunable over 55-63 GHz. With respect to the previous SHIL-QVCO design, the oscillation amplitude is more uniform over the locking range and calibration is facilitated with an envelope detector. The lock detector is constructed around a simple harmonic lock-in amplifier. The large locking range, the large tunability and the combination of envelope detector and lock detector offer a simple approach for robust mm-wave frequency synthesis based on subharmonic injection locking.
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Nomenclature

$Q$ quality factor

**CML** current-mode logic

**DAC** digital-to-analog converter

**FCC** Federal Communications Commission

**IF** intermediate frequency

**ILFD** injection-locked frequency divider

**ILO** injection-locked oscillator

**I/Q** quadrature format

**IRR** image rejection ratio

**ITRS** International Technology Roadmap for Semiconductors

**LD** lock detector

**LO** local oscillator

**LR** locking range

**PCB** printed circuit board

**PLL** phase-locked loop

**PPF** polyphase filter

**QVCO** quadrature voltage-controlled oscillator

**SHILO** subharmonically injection-locked oscillator

**SHIL-QVCO** subharmonically injection-locked QVCO
$\text{SHIL-QVCO}_{W1}$ first realization of a SHIL-QVCO with a wide locking range

$\text{SHIL-QVCO}_{W2}$ second realization of a SHIL-QVCO with a wide locking range

$\text{SNR}$ signal-to-noise ratio

$\text{VCO}$ voltage-controlled oscillator
Chapter 1

Introduction

Researchers in the RF microelectronics have recently been focusing on mm-wave radio circuits. Such high frequencies allow for very appealing applications like high-datarate communication, car radars, imagers and material characterization. Further, the advanced CMOS technology is now capable of mm-wave operation, thus potentially allowing for the realization of low-power low-cost mm-wave devices. For most applications, the state of the art in mm-wave CMOS IC design is not yet ready for an industrial mass production. Furthermore, mm-wave operation in CMOS is possible but still challenging due to some technology limitations. Therefore, mm-wave CMOS design is currently fascinating many researchers in the world, including the author of this Ph.D. dissertation.

1.1 Relevance of mm-wave wireless applications

Mm-wave frequencies are defined as the frequencies whose electromagnetic wavelength ranges from 1 mm to 10 mm in free space, thus ranging from 30 GHz to 300 GHz. Among the various mm-wave applications (Fig. 1.1), some of them require the generation of a stable frequency or a stable time reference. Few examples are:

- 60 GHz communication [Hansen11] [Floyd06]. To enable Gbit/s wireless communication (e.g. for high-definition video link), an unlicensed 7 GHz band has been allocated around 60 GHz. This frequency band is slightly different for Asia, Europe, Australia and America, and the worldwide union of the 7 GHz frequency bands spans the interval from 57 GHz to 66 GHz. Currently, standardization is evolving for these frequency bands. For example, an IEEE working group has elaborated the 802.11ad standard. Examples of applications that are targeted with this standard are the wireless digital data transfer between a high-definition TV (HDTV) and a DVD player of uncompressed high-definition video, wireless docking stations of PCs, fast wireless downloading of several Gbit of data, also called fast Sync & Go.
• **Licensed E-band.** This band is for point-to-point communications, useful for telecommunications backhauls or point-to-point local-area networks. For instance, bands have been set aside in the US at 71-76 GHz, 81-86 GHz, and 92-95 GHz.

• **Vehicular Radar.** The 76-77 GHz band is allocated to forward-looking vehicular radar. Such radars are also called adaptive cruise control or collision avoidance radars, and would provide drivers useful warnings about obstacles on their path. These radars would be an evolutionary step towards intelligent traffic systems. The 77-79 GHz band is allocated for short range vehicular radar.

• **94 GHz Band.** The 94 GHz band could be used for imaging or wireless communications. This band is included in the licensed E-band allocation. Regarding imagers, the wavelength at 94 GHz provides excellent resolution, while many materials, clothes included, are transparent to 94 GHz. This provides an opportunity for various security applications, such as airport screening, provided privacy rights are maintained.

For all the applications mentioned above (high-data rate communication and sensors), mm-wave frequencies are convenient mainly for two reasons: *carrier frequency* and *bandwidth*. The choice of carrier frequency sets the communication channel, with a certain attenuation which depends on the frequency itself. The bandwidth influences the *channel capacity*, as explained below in the text.
Fig. 1.2 shows the atmospheric attenuation, in dB per kilometer, over a frequency range from 10 GHz to visible light. The mm-wave band is colored in green, infrared in red, visible light in blue. Almost all imaging technologies use one of those three bands, X-rays being a notable exception. The red curve shows the total attenuation by the Earth’s atmosphere. It is immediately clear why the human eye is optimized for capturing visible light: because the attenuation is extremely low. At mm-wave frequencies this attenuation is remarkably higher. But, in presence of fog (fog density of 0.1 gram per cubic meter in Fig. 1.2), the optical visibility drops to 50m, being much lower than the mm-wave visibility. In this way, mm-wave car radars can be more reliable than optical radars. Another reason in favor of mm-wave sensors is that mm-wave frequencies can penetrate clothing, whereas light cannot. X-rays can but they raise health issues.

It can be noticed from Fig. 1.2 that, among the mm-wave frequencies, 60 GHz has one of the highest attenuations, around 20 dB/km. In absolute values, such an attenuation is not high and, anyway, is not an issue for short-range and medium-range 60 GHz communication systems.

The second advantage of mm-wave frequencies is the large available bandwidth, at least compared to wireless applications that operate below 10 GHz. In communications, a larger bandwidth enhances the channel capacity, in radar or sensing it results in a higher resolution. The channel capacity $C$ represents the theoretical upper bound on the in-
formation rate (excluding error correcting codes) of clean data that can be sent with a given average signal power $S$ through an analog communication channel subject to additive white Gaussian noise of power $N$. It can be quantified by the Shannon-Hartley theorem [Couch07] [Wikipedia04]:

$$C = B \log_2 \left(1 + \frac{S}{N}\right),$$

(1.1)

where

• $C$ is the channel capacity in bits per second;
• $B$ is the bandwidth of the channel in Hertz (passband bandwidth in case of a modulated signal);
• $S$ is the average received signal power over the bandwidth, measured in Watts;
• $N$ is the average noise or interference power over the bandwidth, measured in Watts;
• $\frac{S}{N}$ is the signal-to-noise ratio (SNR)\(^1\) of the communication signal to the Gaussian noise interference expressed as a linear power ratio (not as logarithmic decibels).

The 60 GHz communication allows for a large channel capacity. For instance, the IEEE 802.11ad standard [IEE14] foresees four communication channels, each one of bandwidth $B=1.76$ GHz. Typically, a wireless communication link allows SNRs ranging from 0 dB to 15 dB\(^2\), thus allowing channel capacities ranging from 1.76 Gbit/s to almost 9 Gbit/s.

Mm-wave systems have larger available bandwidths, with respect to other communication frequencies (mostly below 10 GHz), because of three fundamental reasons. The first reason can be found in the metric called fractional bandwidth. Designing a system that occupies 5% of the carrier frequency is generally equally hard, whether it is at 2 GHz or at 80 GHz. However, at 2 GHz this system will have an absolute bandwidth of only 100 MHz, whereas at 80 GHz it will have 4 GHz of bandwidth.

The second reason resides in the fact that lower frequencies are overcrowded, whereas at mm-wave frequencies the standardization is still evolving. Fig. 1.3a shows the bandwidths which are being considered by the FCC [FCC]:

• 57-66 GHz assigned to high-data rate communication;
• 76-81 GHz worldwide assignment to car radar is evolving;
• 92-100 GHz assigned to radio location;

\(^1\)To be more precise, the measure that really matters is the so called SNDR: ratio of signal power to (noise power plus spurious harmonics power). These spurious harmonics are those appearing in circuit nonlinearities. Since here the propagation through atmosphere is considered, the SNDR is approximated with the SNR.

\(^2\)The communication link is the signal link from transmitter to receiver. The link SNR is mostly limited by the link distance, the antenna’s orientation, the transmitter’s and receiver’s noise floors and the LO phase noise.
1.1 Relevance of mm-wave wireless applications

- 126-142 GHz assigned to radio location.

Fig. 1.3b shows that many standards crowd the spectrum below 6 GHz (e.g. GSM, ATSC, Wimax, WiFi, DECT, DVB, Bluetooth, LTE), whereas - at the moment - at 60 GHz there is only WiGig and at 80 GHz there is only car radar.

The third reason resides in the regulation. A 4 GHz wide band has been assigned to radar in Europe. The car industry is working hard to harmonize the use of this band worldwide, with regulation almost finalized in Japan for instance.
Figure 1.3: Frequency bandwidths available at mm-wave frequencies: (a) bandwidths under consideration of the FCC; (b) larger bandwidths are available at mm-wave frequencies for three reasons: 1) a certain fractional bandwidth (e.g. 5%) is larger at higher carrier frequencies, 2) lower communication frequencies (< 10 GHz) are already crowded by many standards and 3) large bandwidths are being considered for standardization (e.g. a 4 GHz bandwidth around 79 GHz for mm-wave radar in Europe).
1.2 CMOS-based mm-wave frequency synthesis

1.2.1 CMOS technology becomes faster

The commercial success of the different existing wireless communication systems is due to their compactness, their low power consumption and their wide variety of features and functions. These features are enabled by the intensive use of silicon-based microelectronics. The main technology that is used here is CMOS (complementary metal-oxide semiconductor transistors). CMOS is preferred to other faster technologies (such as SiGe) because of the lower cost. This CMOS technology has been downscaled for several decades, enabling the manufacturing of very complex ICs at an affordable price.

![Figure 1.4: Maximum-gain frequency $f_{\text{max}}$ of CMOS and SiGe versus the minimum noise figure $NF_{\text{min}}$ at 60 GHz. Advanced CMOS technology nodes become as fast as SiGe (source: ITRS 2011 [ITRS]).](image)

Currently, CMOS technology has advanced so much that operations at mm-wave frequencies have become feasible [Rieh08]. Fig. 1.4 plots the $f_{\text{max}}$ of some advanced CMOS technology nodes, comparing with a fast technology like SiGe, as predicted by the International Technology Roadmap for Semiconductors (ITRS) [ITRS]. Taking as rule of thumb that, in a given technology, RF circuits can work properly up to $f_{\text{max}}/4$, the latest CMOS technology nodes (such as 40 nm and 28 nm) allow for mm-wave operation.

With the potential of such a high-frequency operation, CMOS technology achieves another advantage for mm-wave applications: it enables the monolithic integration of the digital-rich baseband circuits with RF or mm-wave blocks. This will eliminate the need for an external link, such as wirebonding or flip-chip mounting, between the two blocks, avoiding the degradation of various electrical performances as well as the reliability.

Although modern CMOS allows for mm-wave operation, the fact of using the technology relatively close to its limits (here represented with $f_{\text{max}}$) brings some challenges as
One of the biggest challenges is the availability of accurate device models, both active and passive, at the mm-wave frequency range. The device models provided by the commercial foundries of today for CMOS technology are typically limited up to 20 GHz. This may require the development of in-house models accurate up to mm-wave frequencies. Passive modelling is important as well, since mm-wave wavelengths (between 0.5 mm and 0.5 cm on silicon) become comparable to the circuit size. Accurate passive modelling is usually performed via extensive electromagnetic simulations and, if possible, with measurement verifications.

One key advantage of designing circuits operating at mm-wave frequencies is the smaller dimension required for passive components [Rieh08]. To achieve an impedance of 50 Ω from a purely inductive component at 60 GHz, for example, requires an inductance of only 133 pH, which can be realized with a footprint smaller than 30 by 30 μm² with spiral inductors.

However, there is a critical drawback for having the small values of reactive components corresponding to rather large impedance at the mm-wave frequencies: the effect of parasitic reactive components is seriously magnified. This drastically shrinks the design margin in mm-wave circuit designs, and fabricated circuits will be highly sensitive to any process variation or model mismatch. Hence, a precise extraction and compensation of interconnect parasitics is a vital requirement for the success of mm-wave circuit designs.
1.3 Frequency synthesis at mm-wave

1.3.1 Generalities on frequency synthesis

The frequency synthesizer provides a stable LO signal at the central frequency of the targeted channel. This synthesizer is typically made by putting a voltage-controlled oscillator (VCO) in a PLL [Razavi02], as shown in Fig. 1.5. In a PLL, the phase of the output signal of a (high-frequency) VCO is compared, mostly after frequency division, to the phase of a spectrally pure signal from a crystal oscillator. A very important specification of the LO signal is the phase noise. This phase noise decreases the signal-to-noise-and-distortion ratio in the receiver. A low-phase-noise VCO is often made with a resonant circuit, having a fixed inductor and a tunable capacitor. This resonant circuit, often referred to as the LC tank, must have a high quality factor to allow for a low phase noise.

![Figure 1.5: Basic architecture of a phase-locked loop (PLL).](image)

1.3.2 Frequency synthesis for frequency conversion

The output frequency of the PLL is used to downconvert the high-frequency signal to low frequencies in a receiver or to upconvert a baseband signal to high frequencies in a transmitter. Classical radio architectures perform this frequency conversion in different steps. This is the so-called superheterodyne architecture. In such receivers, the signal is first downconverted to an intermediate frequency (IF) that is usually about one order of magnitude lower than the original carrier frequency. At this IF, an amplification and bandpass filtering are performed after which the signal is further downconverted. Since bandpass filtering is difficult to realize in CMOS technology, the conversion of the wanted signal, from high frequencies to 0 Hz, is performed in one step. This architecture, referred to as zero-IF direct down- and up-conversion (see Fig. 1.6), requires the generation of a high-frequency LO signal ($\cos(\omega_c t)$ in Fig. 1.6, where $\omega_c$ is equal to the carrier frequency) together with a 90-degrees shifted replica ($\sin(\omega_c t)$ in Fig. 1.6). This combination of signals is called a quadrature signal.
1.3.3 Generation of quadrature-LO signals at mm-wave

For wireless communication applications below 10 GHz, the generation of quadrature-LO signals is typically performed by combining a PLL at double the frequency with a master-slave static frequency divider. Such a divider produces two signals that are shifted by 90 degrees with respect to each other. For mm-wave operation, for instance at 60 GHz, this approach would require a frequency divider and a VCO operating at 120 GHz. This frequency is too demanding for the advanced CMOS nodes of today. Therefore, alternatives must be found to generate quadrature-LO signals at mm-wave.

One possible solution is the use of a so-called quadrature voltage-controlled oscillator (QVCO). This produces four outputs which are each shifted in phase by 90 degrees. A classic LC QVCO is shown in Fig. 1.7: it consists of two differential LC VCOs, coupled to each other through transconductors. Thanks to this coupling, the two locked oscillators find a common frequency, which can slightly differ from the free-running frequency of the single oscillators themselves [Mirzaei07]. The configuration shown in Fig. 1.7 is called parallel QVCO because the two coupling transistors are in parallel with the active core of each of the two VCOs.

A QVCO can suffer from mismatch. If the two oscillators match perfectly, their output phases are in precise quadrature. However, mismatches in the circuit components cause the outputs to depart from quadrature.

A further issue of QVCOS is the mode ambiguity [Mirzaei07]. A QVCO can oscillate in more than one mode. Each mode is characterized by a different phase shift between the two VCOs constituting the QVCO. The mode with phase shift of +90° and the mode with
1.3 Frequency synthesis at mm-wave

phase shift of \(-90^\circ\) are the only ones to be stable. According to the QVCO topology, one mode is always stable and the other one is conditionally stable. This stability condition depends on the phase introduced by the coupling between the two VCOs. Therefore, the mode ambiguity can be solved by introducing a particular phase delay in the coupling between the two VCOs. If not solved, the mode ambiguity is dangerous because, the QVCO driving a complex mixer, it cannot be guaranteed whether the mixer will select the upper or the lower sideband.

1.3.4 Injection locking for mm-wave frequency synthesis

Mm-wave operation with advanced digital CMOS nodes is feasible but still challenging. Traditional circuit topologies used for lower-frequency communication (< 10 GHz) ported to mm-wave frequencies (e.g. for 60 GHz communication) typically either do not work properly or require a large power consumption.

One example of such critical circuits, in the context of frequency synthesis, is the frequency divider of a mm-wave PLL. According to what is done at lower frequencies (below 10 GHz), a mm-wave PLL would be implemented as depicted in Fig. 1.8a: the output of a high-frequency VCO would be monitored with frequency dividers. Typically, static frequency dividers are implemented with CML latches. Apart from [Szortyka14] - which has been very recently published - no published mm-wave PLL uses static dividers at mm-wave because of the large power consumption they would require at such high frequencies. The designs in this Ph.D. work were mainly based on the 40 nm low-power tech-
nology, which is slower than the 40 nm general-purpose technology used in [Szortyka14].

The use of the static divider of that work is not possible in 40 nm low-power. With the availability of faster technologies (40 nm general-purpose, 28 nm and beyond), the results of this work are more relevant for mm-wave applications at frequencies above 60 GHz.

![Diagram of mm-wave PLL](image)

**Figure 1.8:** Possible implementations of a mm-wave PLL: (a) with a static frequency divider (e.g. CML latches); (b) with the combination of an ILFD (for high-frequency division) and a static divider (for low-frequency division); (c) with a high-frequency SHILO locked to a lower-frequency PLL.

Alternative circuit topologies can relax the mm-wave frequency division thanks to the use of injection-locking techniques. Injection locking allows for high-frequency operations with a relatively low power consumption. The basic principle of injection-locking techniques is the synchronization of an oscillatory system with an external signal. Such a synchronization can occur on the frequency of the external signal, on a multiple of this frequency or on a submultiple of this frequency. In this way, frequency multiplication or frequency division can be realized. In the context of mm-wave frequency synthesis, two main applications of injection locking are mm-wave injection-locked frequency dividers and mm-wave subharmonically injection-locked oscillators.
An injection-locked frequency divider (ILFD), for instance in a 60 GHz PLL, consists of an oscillator, running at $60/n$ GHz ($n$ integer), synchronized to the 60 GHz signal coming from the oscillator. A mm-wave PLL, using an ILFD for high-frequency division, would look like depicted in Fig. 1.8b. Examples of such mm-wave PLLs are [Shima11], [Tabesh11] and [Vidojkovic13a].

A subharmonically injection-locked oscillator (SHILO), running for instance at 60 GHz, consists of a 60 GHz oscillator synchronized to a $60/n$ GHz ($n$ integer) signal coming from a $60/n$ GHz ($n$ integer) PLL. In this case, thanks to the frequency multiplication from $60/n$ GHz to 60 GHz, the use of mm-wave dividers is avoided, as depicted in Fig. 1.8c. Examples of such an approach are [Chan10], [Okada11], [Vidojkovic12] and [Raczkowski12].
1.4 Objectives and outline of this work

The scope of this Ph.D. work is to investigate, design and verify some (possibly novel) injection-locking techniques for mm-wave frequency synthesis in CMOS. This Ph.D. has been conducted in collaboration with imec, Belgium, where mm-wave research is focusing on 60GHz communication and (only recently) on 79 GHz automotive radars. Therefore, this Ph.D. has focused on the 60 GHz application.

This thesis is organized as follows:

- Chapter 2 introduces injection locking, together with the two main techniques used for frequency synthesis: *frequency multiplication* and *frequency division*.

- Chapter 3 focuses on an inductor-less 60-15 GHz ILFD in 40 nm CMOS, integrated in a 60 GHz PLL. Such a topology is widely used in state of the art, but it suffers from a high power-supply sensitivity. In this work, this issue is recognized in simulations and tackled with a dedicated design.

- Chapter 4 focuses on a 60 GHz LO system, based on subharmonic injection locking, and integrated in a four-path phased array receiver in 90 nm CMOS. This LO system demonstrates the feasibility of subharmonic injection locking for mm-wave frequency synthesis and enhances the RF design modularity: all the 60 GHz circuitry is restricted into a small area on chip.

- Chapter 5 focuses on a novel use of coupled-LC tanks for SHILOs. Such an approach significantly enhances the locking range. A large LR is beneficial because it facilitates the system calibration and makes the lock more robust against disturbances. This approach is demonstrated on two 60 GHz SHIL-QVCOs in 40 nm CMOS.

- Chapter 6 focuses on a lock detection mechanism, which is simpler than other state-of-the-art solutions. Lock is detected with a simple circuit (basically a lock-in amplifier) giving a DC output. Furthermore, a simple calibration procedure is proposed for coupled-LC-tank SHILOs, which involves only DC measurements, hence no frequency measurement is needed.

Although this Ph.D. has focused only on 60 GHz frequency synthesis, the findings are useful for any other mm-wave carrier frequency synthesized in CMOS. The main achievements and the outlook of this Ph.D. work are discussed in Chapter 7.

---

3 The locking range, defined as the frequency range over which the SHILO can be locked, is introduced in Chapter 2.
Chapter 2

Injection locking for frequency synthesis in CMOS

2.1 Introduction

Injection-locking techniques allow for circuit operation at mm-wave frequencies with relatively low power consumptions. The key principle of such techniques is that an oscillator is synchronized to the frequency of an external injected signal. Such a synchronization can occur on the frequency itself or on a multiple or on a submultiple of that frequency.

Two main applications of injection locking for 60 GHz frequency synthesis are mm-wave injection-locked frequency dividers and mm-wave subharmonically injection-locked oscillators. The former consists of an oscillator, running at 60/n GHz (n integer) and used as frequency divider, synchronized to the 60GHz signal coming from the 60 GHz oscillator. The latter consists of a 60 GHz oscillator, used as frequency multiplier, synchronized to a 60/n GHz (n integer) signal coming from a 60/n GHz PLL. In this last case, thanks to the frequency multiplication from 60/n GHz to 60 GHz, the use of mm-wave frequency dividers is avoided.

The advantage of injection locking is often paid with a lack of robustness of the system. For instance, injection-locked frequency dividers are sensitive to supply disturbances², thus endangering the robustness of the PLL operation. Mm-wave subharmonically injection-locked oscillators often can be locked only over a narrow frequency range. In other words, they offer a narrow locking range. Consequently, the injection-locked oscillator needs to be accurately tuned so that the narrow locking range is centered at the targeted frequency. Furthermore, disturbances can easily bring such an oscillator out of lock³.

¹From now on, this text will focus on the 60 GHz communication as representing a mm-wave application. ²In the remainder of this text this is proven with simulations. ³A subharmonically injection-locked oscillator can be seen as a frequency-locked loop. A narrow locking
In this context, a key point for a robust design requires to understand the basic principles of injection locking. Thanks to this, the circuit can be designed such that the locking range is large enough for a robust operation and the supply sensitivity of dividers can be reduced. Session 2.2 illustrates the basic principles of injection locking, focusing on the frequency multiplication and the frequency division. Section 2.3 gives general remarks for RF CMOS designs based on injection locking and section 2.4 draws conclusions.
2.2 Basic principles of injection locking

The basic principle of injection locking is the synchronization of an oscillatory system with an external signal. Such a phenomenon has been extensively studied for electronic circuits, e.g. in [Adler46], [Razavi04], [Mirzaei07] and [Lee09]. If the external signal’s frequency is similar to the oscillator’s fundamental frequency, the oscillator locks to the external frequency and the output close-in phase noise is shaped by the external signal. As mentioned above, this technique allows for circuit operation at high frequencies (such as mm-wave) with a low power consumption. The challenge - and the charm as well - of injection locking resides in the fact that we want to synchronize, with an external signal, the oscillatory response of an unstable system such as an oscillator.

2.2.1 Locking range

An important parameter of an injection-locked oscillator (ILO) is the locking range (LR). It is defined as the frequency range over which the oscillator locks to the external injected signal. If the external signal’s frequency falls out of this range, the oscillator is not locked and undergoes some pulling phenomena [Razavi04]. Fig 2.1 depicts the output frequency of an injection locked oscillator in dependence of the injected frequency, thus showing the LR.

![Figure 2.1: Output frequency of an injection-locked oscillator versus the injected signal’s frequency. The LR is defined as the frequency range over which the oscillator is locked to the input frequency.](image)

Simple models of an ILO are present in literature, which relate the LR to circuit parameters and the to injected input power. Although such models are approximate, they provide insight and thus are useful for the circuit design. Similarly to [Razavi04] and [Mirzaei07], the ILO is modelled as depicted in Fig. 2.2(a): a resonant tank together with an active core. The active core consists of a negative conductance $G_m$ and a current source as external signal injection $I_{inj}$. Hence,

$$\vec{I}_{\text{tank}} = \vec{I}_{\text{osc}} + \vec{I}_{\text{inj}}, \tag{2.1}$$
Figure 2.2: (a) General model for an ILO. (b) Phasor diagram. (c) Limit for $\alpha$: given $|I_{\text{osc}}|$ and $|I_{\text{inj}}|$, $\alpha$ must be inferior or equal to $\alpha_{\text{lock}}$.

where

$$\vec{I}_{\text{osc}} = G_m \vec{V}_{\text{osc}}.$$  \hfill (2.2)

Defining $Z_{\text{tank}}$ as the resonant tank’s impedance seen by the active core, we have:

$$\vec{V}_{\text{osc}} = Z_{\text{tank}} \vec{I}_{\text{tank}}.$$  \hfill (2.3)

Assuming that all the phasors turn at the same frequency, a phasor diagram of (2.1) can be drawn as in Fig. 2.2(b), where $\alpha$ is defined as the phase difference between $\vec{I}_{\text{tank}}$ and $\vec{I}_{\text{osc}}$:

$$\alpha = \angle \vec{I}_{\text{tank}} - \angle \vec{I}_{\text{osc}}.$$  \hfill (2.4)

Combining (2.2), (2.3) and (2.4) and assuming $G_m$ to be a real number, implies:

$$\alpha = -\angle Z_{\text{tank}}.$$  \hfill (2.5)

Hence, $\alpha$ is found to be equal (apart for the sign) to the phase of the resonant tank impedance. In other words, if the oscillator is locked at a frequency at which $\angle Z_{\text{tank}} \neq 0$, $I_{\text{inj}}$ must compensate for the consequent phase difference between $I_{\text{tank}}$ and $I_{\text{osc}}$. For given $|I_{\text{osc}}|$ and $|I_{\text{inj}}|$, the maximum phase shift that can be compensated is: 

$$\alpha_{\text{lock}} = \arcsin \left( \frac{|I_{\text{inj}}|}{|I_{\text{osc}}|} \right).$$  \hfill (2.6)

In this case $I_{\text{inj}}$ is orthogonal to $I_{\text{tank}}$ (Fig. 2.2.c). If at a certain frequency $\alpha > \alpha_{\text{lock}}$, such phase shift can no longer be compensated and therefore injection locking cannot
2.2 Basic principles of injection locking

occur. Notice that in this context it is assumed that $|I_{\text{inj}}| < |I_{\text{osc}}|$, which is usually the case for an ILO.

Combining (2.6) with (2.2) and (2.5), the condition for injection locking can be expressed in terms of circuit parameters:

$$|\angle Z_{\text{tank}}(\omega)| \leq \arcsin \left( \frac{|I_{\text{inj}}|}{G_m|V_{\text{osc}}|} \right).$$  \hspace{1cm} (2.7)

As a result, the LR can be defined as the frequency range over which (2.7) is valid:

$$LR = \{\omega : |\angle Z_{\text{tank}}(\omega)| \leq \alpha_{\text{lock}}\}.$$  \hspace{1cm} (2.8)

**Single-resonance LC-tank ILO**

Figure 2.3: Simplified model of an ILO with a single-resonance LC tank.

Most mm-wave ILOs are single-resonance LC-tank oscillators. Such ILOs can be modelled as depicted in Fig. 2.3 and its LR equals [Razavi04]:

$$LR = \frac{\omega_0}{Q} \frac{I_{\text{inj}}}{I_{\text{osc}}} \frac{1}{\sqrt{1 - \left(\frac{I_{\text{inj}}}{I_{\text{osc}}}\right)^2}},$$  \hspace{1cm} (2.9)

where $\omega_0 = 1/\sqrt{LC}$ is the LC-tank self-resonance frequency, $Q$ is the LC-tank quality factor and is related to $\alpha$ with [Razavi04]:

$$\tan(\alpha) \approx \frac{2Q}{\omega_0} (\omega_0 - \omega_{\text{inj}}).$$  \hspace{1cm} (2.10)

**Design considerations**

Referring to (2.7), (2.8) and (2.9), the LR can be extended by:

- Increasing the injected current $I_{\text{inj}}$. This typically comes with a higher power consumption.
- Reducing $G_m$, but a minimum $G_m$ is required to ensure oscillation.
- Lowering the $Q$ of the resonant tank. This typically comes with a lower oscillation amplitude $|V_{\text{osc}}|$ for a given current $|I_{\text{tank}}|$, thus lowering the system efficiency.
Such considerations represent a starting point for a design based on injection locking. They also represent the limits to the system performance (e.g. LR versus oscillation amplitude or LR versus power consumption).

2.2.2 Phase-noise shaping

One of the main benefits of injection locking is the phase-noise shaping: the phase noise of an ILO can be reduced by injection locking to a low-noise source [Razavi04]. From a time-domain perspective, the synchronizing effect of injection manifests itself as correction of the oscillator zero crossings in every period, thereby lowering phase noise. It is demonstrated in [Razavi04] that the reduction of phase noise is maximum when the injected frequency resides at the center of the LR (where the zero crossings of $I_{\text{inj}}$ greatly impact those of $I_{\text{osc}}$) and minimum when operating at the LR’s edges (where the zero crossings of $I_{\text{inj}}$ coincide with the zero-slope points on $I_{\text{osc}}$, since $\vec{I}_{\text{inj}}$ and $\vec{I}_{\text{osc}}$ are orthogonal to each other, as in Fig. 2.2.c). Thus, the phase noise profile of the free-running ILO (i.e., no signal injected) and the phase noise profile of the locked ILO meet at the edges of the LR, as depicted in Fig. 2.4. In addition to this model, reference [Chen08] stresses that the locked close-in phase noise is dictated not only by the external signal’s phase noise but also by the noise added by the injecting circuitry as well.

![Figure 2.4: Phase noise of an ILO in free running (gray line) and in injection locking (black line). The ILO’s free-running oscillation frequency is $\omega_0$, which coincides here with the center of LR. The injection is assumed to be at $\omega_0$ as well. The LR ranges from $\omega_0 - \omega_L$ to $\omega_0 + \omega_L$ (figure copied from [Razavi04]).](image)

2.2.3 Frequency multiplication

An ILO can lock to the $n$-th harmonic of the external injected signal. In this case, we talk about subharmonic injection locking. It can be seen like a sort of frequency multiplication.
2.2 Basic principles of injection locking

Under lock, the ILO’s phase noise is then mainly dictated by the injected signal. Since the output frequency is $n$ times the input frequency, the close-in output phase noise is then equal to $n^2$ times the input phase noise [Lee09]. Fig. 2.5 depicts the phase noise of a subharmonically injection-locked oscillator (SHILO) when locked to the $n$-th harmonic of a lower-frequency PLL signal. Thanks to the phase-noise shaping, a mm-wave SHILO locked to a lower-frequency PLL can perform comparably or even better than a mm-wave PLL. In a mm-wave PLL, the out-of-band phase noise is determined by the passives of the mm-wave oscillator, which typically have a low quality factor at mm-wave [Chan08] [Musa11].

Figure 2.5: Phase noise of a SHILO (figure adapted from [Lee09]). Under lock, the in-locking-band phase noise follows the phase noise of the injected signal with a factor of $N^2 (20\log_{10} N)$ in dB).

Apart from the phase-noise shaping, subharmonic injection locking can bring other benefits for mm-wave frequency synthesis. Fig. 2.6 depicts an example of 60 GHz LO system based on subharmonic injection locking. Typically, 60 GHz radios perform beam-forming to improve the link budget and therefore more than one RF front-end are present on the chip. With respect to the traditional case of a 60 GHz PLL, the advantages of the system in Fig. 2.6 are:

- no mm-wave frequency dividers are required since the PLL operates at a lower frequency;
- a lower frequency is distributed to the various front-ends;
- the whole 60 GHz circuitry can be positioned close to the front-end, thus improving the design modularity.

Locking range of a SHILO

The main challenge in a SHILO is to obtain a sufficiently wide LR. Subharmonic injection locking relies on the $n$-th harmonic of the injected signal. References [Zhang92] and
[Kanemaru11] give an approximate expression\footnote{In [Zhang92] and [Kanemaru11] there is a factor $\frac{1}{2}$ since they consider the single-sideband LR, whereas in this text we consider the double-sideband LR.} for the LR of a SHILO, which resembles (2.9):

$$LR = \frac{\omega_0}{Q} \sqrt{\frac{P_{inj,n}}{P_0}}, \quad (2.11)$$

where $P_{inj,n}$ is the $n$-th harmonic power of the reference signal and $P_0$ is the free-running output power of the oscillator. Such $n$-th harmonic $P_{inj,n}$ is generated thanks to the nonlinearities present in the circuit. Some enhancement of the LR can be achieved by enhancing the circuit nonlinearities [Chen08].

Typically the LR becomes narrower with a higher order $n$ of subharmonic injection, due to the fact that $P_{inj,n}$ is lower for higher $n$. For instance, supposing that a sinusoidal subharmonic signal is injected into the SHILO, and supposing that the circuit nonlinearities distort such a sinusoidal signal into a square wave, the generated $n$-th harmonic is smaller for higher $n$, as from the Fourier series of a square wave comes that:

$$P_{inj,n} \propto \left\{\sin\left(\frac{\pi n}{\pi n}\right)\right\}^2. \quad (2.12)$$

The narrow LR of a SHILO can be extended by compromising the system performance, as mentioned in the design considerations of Subsection 2.2.1. Chapter 5 will deal with a novel approach for extending the LR without heavily compromising the system efficiency.

### 2.2.4 Frequency division

Injection locking can be used for frequency division: an oscillator is synchronized to a submultiple of the injected signal’s frequency. A injection-locked frequency divider
(ILFD) is modelled in Fig. 2.7a: the $(n-1)$-th harmonic of the oscillator, i.e. $(n-1)f_{osc}$, beats with the injected signal, $f_{inj}$, and the resulting beat frequency, $f_{inj} - (n-1)f_{osc}$, is injected back into the oscillator. Such a beat frequency pulls the oscillator (Fig. 2.7b), resulting in $f_{osc} = f_{inj}/n$. An alternative model replaces the $(n-1)$-th harmonic with the $(n+1)$-th harmonic (Fig. 2.7c).

![Diagram](image)

**Figure 2.7:** Injection-locked divide-by-$n$ (figure copied from [Mirzaei08]). (a) The $(n-1)$-th harmonic of the oscillator beats with the injected signal and the resulting beat frequency is injected back to the oscillator. (b) The beat frequency pulls the oscillator. (c) Same model as in (a) but with the $(n+1)$-th harmonic instead of the $(n-1)$-th harmonic.

ILFDs present advantages and disadvantages with respect to classical static logic dividers. ILFDs can work at mm-wave frequencies, consuming a lower power than logic dividers do at mm-wave. On the other hand, logic dividers can operate over a much wider frequency band while the ILFDs need to be calibrated so that their LR covers the targeted frequency. Therefore, ILFDs are typically used only when static logic dividers cannot, like for the high-frequency division in a high-frequency PLL (Fig. 2.8).
Figure 2.8: Block diagram of a high-frequency PLL using an ILFD for high-frequency division and static latches for the lower-frequency division.
2.3 General design remarks

Because of the high-frequency, mm-wave CMOS circuits need to be designed with a hybrid approach that uses both *lumped parameters* and *distributed parameters*. Indeed, simulations have shown that metal interconnections with a length above 10 µm are best represented as transmission lines rather than a capacitance to ground or a series resistance and shunt capacitance. Resonances at mm-wave frequencies are very sensitive to parasitic capacitances of a few femtoFarad and therefore passive components - such as inductors and transformers - need to be accurately designed and simulated together with the surrounding environment (e.g. ground walls and planes, slots, bends etc.).

Subharmonic injection locking requires further points of attention. For instance, the frequency multiplication and division - described previously - rely on nonlinearities. Such nonlinearities are not always well modelled in the MOS transistor models, especially for mm-wave frequencies and digital CMOS technologies. Hence, the LR obtained in measurements can differ from the LR achieved in simulations. Another point of attention is the quality factor of passives, which strongly affects the LR (see Chapter 5).

The simulation of injection-locked circuits described in this Ph.D. challenges the designer, since the output frequency cannot be easily predicted if the system is out of lock. This is the reason why the circuits described in this work have been mainly simulated with bare transient simulations. Only if the system is surely in lock, analysis techniques such as *periodic-steady-state* analysis and *harmonic-balance* analysis produce reliable results.

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5The wavelength of 60 GHz is 5 mm in air and about 2.5 mm on silicon. Therefore, the circuit dimensions become comparable with the wavelength.
2.4 Conclusions

Injection-locking techniques are interesting for mm-wave frequency synthesis in CMOS. They allow for high-frequency operations with relatively low power consumption. The key principle of such techniques is that an oscillatory circuit is synchronized to the frequency of an external injected signal. Such a synchronization can also occur on the $n^{th}$ harmonic of the injected signal’s frequency, thus realizing a sort of frequency multiplication. The synchronization can also occur on the $n$-th submultiple of the injected signal’s frequency, thus realizing a frequency division.

Two main applications of injection locking for mm-wave frequency synthesis are mm-wave injection-locked frequency dividers (ILFDs) and mm-wave subharmonically injection-locked oscillators (SHILOs). ILFDs allow for mm-wave frequency division in a mm-wave PLL (Fig. 2.8). SHILOs allow for the use of a lower-frequency - and thus less complex - PLL, a lower-frequency LO distribution and a more modular mm-wave RF design (Fig. 2.6). Another advantage of SHILOs is phase-noise shaping. Thanks to this, mm-wave SHILOs, locked to a lower-frequency PLL, can perform comparably or even better than mm-wave PLLs.

CMOS RF circuit design, at mm-wave frequencies and based on injection locking, requires particular attention. Because of the high operating frequency, the design approach must be a sort of hybrid between lumped parameters and distributed parameters. Further, a reliable simulation of injection-locked systems requires a good modelling of nonlinearities and a good estimation of the quality factor of passives.

The main challenge of injection-locked systems is the locking range (LR). It is defined as the frequency range over which the system can be locked. If the LR is narrow, the system needs to be accurately tuned so that the narrow LR is centered at the targeted frequency. Further, disturbances can easily bring the system out of lock. Therefore a large LR is preferred for a robust operation. The LR can generally be enhanced by compromising the power consumption or the signal amplitude, thus lowering the system efficiency. Such trade-offs are experimentally verified in Chapter 4. A novel approach for enhancing the LR, without heavily lowering the system efficiency, is described and verified in Chapter 5.
Chapter 3

Injection-locked frequency division

3.1 Introduction

In the last years the research of CMOS-based mm-wave frequency synthesis has been focusing on mm-wave phase-locked loops (PLLs), where the mm-wave frequency division is one of the most challenging operations. At lower frequencies, static CML latches are used for frequency division, but their power dissipation at mm-wave becomes unacceptably large. For this reason, the high-frequency division must be performed by a dedicated high-frequency prescaler, as depicted in Fig. 3.1.

![Figure 3.1: Block diagram of a high-frequency PLL using a high-frequency divider.](image)

ILFDs are widely used for the first divider stage as a mm-wave prescaler. LC-based ILFDs are most common [Mayr07] [Chen09] [Yin12]. They have a low power consumption but occupy a large silicon area. Furthermore, they complicate the RF design flow.

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1The situation can become less dramatic with the next advanced CMOS nodes, given that the transition frequency is higher than it is in the current CMOS nodes.
since the inductors and the capacitors need to match the operation at mm-wave frequencies, where the capacitances of the resonator become comparable to the parasitic capacitance of the active devices.

Inductor-less mm-wave ILFDs are compact, save power consumption and can be tuned over a wide frequency range [Hoshino07] [Decanis11]. They are implemented as injection-locked ring oscillators, where the oscillation frequency is locked to one submultiple of the injected frequency. In [Hoshino07] the prescaler is realized as a three-stage ring oscillator, where the mm-wave signal is injected into the first and the second stages. In [Decanis11] the ring oscillator has four stages and the mm-wave signal is injected into each stage.

Starting from the circuit topologies of [Hoshino07] and [Decanis11], this Ph.D. work has investigated and designed a 60 GHz divide-by-4 prescaler as a part of a 60 GHz PLL. This PLL has been integrated in two 60 GHz four-path phased array radios (transmitter and receiver) [Vidojkovic13a] [Vidojkovic13b]. Compared to the circuit topologies of [Hoshino07] and [Decanis11], simulations show that the solution proposed in this work is more robust against power-supply disturbances. Such a robustness is very important for a proper PLL operation in an entire radio.
3.2 A 60 GHz injection-locked inductorless divider-by-4 in 40 nm CMOS

3.2.1 System overview: a 60 GHz PLL for phased array radios

A 60 GHz PLL has been designed in a 40 nm low-power digital CMOS technology. A block diagram is shown in Fig. 3.2. The frequency division is realized with three circuits: a 60-15 GHz prescaler, a divide-by-2 static divider and a programmable divide-by-N logic divider. In order to cover the whole 60 GHz frequency band, two 60 GHz QVCOs are used (a high-band one and a low-band one). This PLL has been integrated in a 60 GHz four-path phased array transmitter and in a 60 GHz four-path phased array receiver, shown in Fig. 3.3. Such radios allow for a 60 GHz communication link, as published in [Vidojkovic13a] and [Vidojkovic13b]. The scope of this Ph.D. work is put on the 60-15 GHz prescaler, as discussed in the following subsections.

![Block diagram of the 60 GHz PLL](image)

Figure 3.2: Block diagram of the 60 GHz PLL. The 60-15 GHz prescaler is a very critical block.

Contributions of this Ph.D. work

This Ph.D. has investigated, designed and measured the 60-15 GHz prescaler.
Figure 3.3: Micrographs of the 40 nm 60 GHz radios where the 60 GHz PLL is integrated: (a) four-antenna phased array transmitter (6 mm^2), (b) four-antenna phased array receiver (6.5 mm^2).
3.2.2 Investigation and design of the prescaler

Previous design: three-stage injection-locked ring oscillator

In this Ph.D. a 60-15 GHz prescaler has been designed starting from a previous implementation, which is published in [Parvais10]. A circuit schematic of the original design is shown in Fig. 3.4. It is a three-stage injection-locked ring oscillator, based on the design as proposed in [Hoshino07]. The delay cell is a differential pair with an active PMOS load used for frequency tuning. The 60 GHz signal is injected through the tail current source of the first and the second active stages. The frequency tuning is needed such that the LR covers the targeted frequency. The PMOS load consists of a binary-weighted bank of PMOS-triode resistors. Each PMOS-triode resistor can be switched between an on state and an off state by biasing the PMOS gate either to a low voltage or to a high voltage. These two reference voltages - $V_{DACL}$ and $V_{DACH}$ in Fig. 3.4 - come from on-chip digital-to-analog converters.

In this kind of prescalers, the frequency division by four relies on harmonic mixing. The third harmonic of the oscillation signal of the ring oscillator (3× 15 GHz in this context) mixes with the injected signal (60 GHz), to produce an output at one fourth of the injected frequency (15 GHz).

As shown below in the text, this design offers a decent input LR (more than 2 GHz) but it is sensitive to supply disturbances. This sensitivity becomes critical for a robust operation of the PLL, especially when the PLL is integrated in a phased-array radio, where the different circuits may cause various disturbances and supply bounces.
Current design: four-stage injection-locked ring oscillator

A new prescaler design has been investigated starting from the three-stage ring oscillator described above. A four-stage topology of ring oscillator has been chosen because, for a frequency division by four, it is more suitable than the three-stage topology is. In a four-stage topology, the 60 GHz signal can be injected in phase with the 15 GHz oscillation signal of the ring oscillator, as depicted in Fig. 3.5: the 180° phase difference of the 60 GHz differential signal matches with the 45° phase delay at 15 GHz inherently present in the delay stage of the ring oscillator. This improves the efficiency of injection locking, consequently enhancing the LR [Mirzaei08].

A four-stage ring oscillator, with a delay cell that is very similar to the one in Fig. 3.4, has been investigated first. Such a design is depicted in Fig. 3.6 where it is denoted as type A. It is similar to the design proposed in [Decanis11]. As described below in the text, simulations show a large input LR but a visible sensitivity to supply disturbances as well.

Seeking robustness against supply disturbances, a second type of delay cell has been investigated, shown in Fig. 3.6 and denoted as type B. The only difference with type A is the load of the differential pair: the new design has a hybrid load consisting of a differential PMOS-triode resistor connected between the two differential output nodes and two polysilicon resistors connecting the output nodes to the power-supply node.

The power-supply sensitivity is evaluated considering a static disturbance and a dynamic disturbance. Fig. 3.7 shows the simulated input LR of the three-stage prescaler, the four-stage type A prescaler and the four-stage type B prescaler, in the presence of a static supply disturbance. The type A prescaler offers the largest input LR, larger than 5 GHz, against the 2.5 GHz LR of the three-stage prescaler and the type B prescaler. But the type A prescaler, together with the three-stage one, is more sensitive to the supply than the type
A 60 GHz injection-locked inductorless divider-by-4 in 40 nm CMOS

3.2 A 60 GHz injection-locked inductorless divider-by-4 in 40 nm CMOS

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such a sensitivity is evaluated as the frequency shift of the LR with respect to the static supply variation, resulting in:

- three-stage prescaler → $\frac{\Delta f}{\Delta V_{DD}}_{60 \text{ GHz}} \approx \frac{2.25 \text{ GHz}}{10 \text{ mV}}$;
- four-stage type A prescaler → $\frac{\Delta f}{\Delta V_{DD}}_{60 \text{ GHz}} \approx \frac{0.92 \text{ GHz}}{10 \text{ mV}}$;
- four-stage type B prescaler → $\frac{\Delta f}{\Delta V_{DD}}_{60 \text{ GHz}} \approx \frac{0.26 \text{ GHz}}{10 \text{ mV}}$.

Fig. 3.8 and Fig. 3.9 show the simulated output spectrum of the three types of prescaler when a dynamic supply disturbance is applied: a sinusoidal disturbance of 10 mVpk at 100 MHz. These results come from fast-Fourier-transform analysis of transient simulation results. Fig. 3.8 shows that the three-stage prescaler is significantly affected, with many spurs at frequency offsets multiple of 100 MHz. Fig. 3.9, in comparison with Fig. 3.8, shows that the four-stage prescaler is more robust than the three-stage prescaler. Further, the type B prescaler performs better than type A since the 100 MHz-offset spurs are less pronounced ($-36.6 \text{ dBc/Hz}$ against $-25.5 \text{ dBc/Hz}$).

\[ ^{2} \text{To limit the total simulation time, the transient simulation has been set to accommodate a fast-Fourier-transform frequency resolution not lower than 50 MHz.} \]
Figure 3.6: Block diagram of the prescaler (four-stage ring oscillator) and schematic of two types of active stage: type A as a differential pair with active PMOS load and type B as a differential pair with a hybrid load (PMOS load for frequency tuning and polysilicon resistors as static load).
Figure 3.7: LR of the different types of prescaler in dependence of the supply voltage. The four-stage type B prescaler is less sensitive to supply variations than both the three-stage and the four-stage type A prescalers are.

Figure 3.8: Output spectrum of the 3-stage prescaler when a 10 mVpk 100 MHz sinusoidal disturbance is applied to the supply. In addition to the 15 GHz fundamental, many considerable spurs appear at offset frequencies multiples of 100 MHz.
Figure 3.9: Output spectrum of the 4-stage prescaler when a 10 mVpk 100 MHz sinusoidal disturbance is applied to the supply (here the fundamental is 15.25 GHz). Prescaler type B appears more robust than type A since the 100 MHz-offset spurs are lower.
3.2 A 60 GHz injection-locked inductorless divider-by-4 in 40 nm CMOS

3.2.3 Measurement results

The results reported here have been obtained from measurements on the 60 GHz transmitter and the 60 GHz receiver of Fig. 3.3. These chips have been mounted on dedicated PCBs, with all the low-frequency IO pads bonded with the PCB connections and the 60 GHz IO pads left free for on-chip probing. The setups for the receiver and the transmitter measurements are depicted in Fig. 3.10 and Fig. 3.11 respectively. The frequency response of the prescaler has been derived by measuring the PLL divided output frequency. A list of the most important measurement equipment consists of:

- 60 GHz RF spectrum analyzer (Rohde&Schwarz FSU67GHz),
- 67 GHz signal generator (Agilent E 8257D),
- signal analyzer for phase-noise measurements (AGT 5052B),
- low-frequency signal generator for the PLL reference signal (out of the scope of this text),
- arbitrary waveform generator for the transmitter baseband signal (out of the scope of this text).

The prescaler consumes 12mW (under 1.1V supply voltage) and offers an input LR of 2 GHz, corresponding to 0.5 GHz LR at 15 GHz. Fig. 3.12 shows an example of the measured LR, where the 60 GHz QVCO frequency is swept and the prescaler’s oscillation frequency is observed.

Since the input LR is only 2 GHz, it needs to be moved over frequency in order to cover the whole frequency band of interest. This frequency tuning is possible thanks to the binary-weighted bank of PMOS-triode resistors. As explained in Subsection 3.2.2, each PMOS-triode resistor can be switched between an on state and an off state by biasing the PMOS gate either to a low voltage or to a high voltage. Fig. 3.13 shows the prescaler’s free-running oscillation frequency, tuned over the full scale of the PMOS load bank. Different settings of $V_{DACL}$ (setting the low PMOS gate voltage) and $V_{DACH}$ (setting the high PMOS gate voltage) give different tuning ranges. The voltage $V_{DACL}$ influences the upper limit of the tuning range while $V_{DACH}$ influences the lower limit of the tuning range, since $V_{DACH} > V_{DACL}$.

Thanks to such a frequency tuning, the LR can be moved over frequency as shown in Fig. 3.14. It can be observed that the LR is larger when moved to lower frequencies. This is due to the more enhanced nonlinearity in the PMOS-triode bank. More specifically, moving the LR to lower frequencies means biasing more PMOS-triode units with their gate to the high voltage instead of the low voltage. Consequently, more PMOS units are biased with a gate voltage which is closer to the supply voltage and hence more PMOS-triode units are biased with a gate-bulk voltage closer to the threshold. This enhances the nonlinear behaviour of the PMOS-triode resistor and therefore facilitates the harmonic mixing which allows the frequency division of the prescaler. Consequently, the LR is enhanced.

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3The complete measurement setup includes also a number of DC sources, a computer, cables and instrumentation amplifiers. Most of the equipment is remotely controlled with the industry-standard GPIB bus.
Figure 3.10: Measurement setup with the 60 GHz receiver. The prescaler oscillation frequency is derived by measuring the PLL divided output frequency.

Fig. 3.15 reports the prescaler’s free-running oscillation frequency measured at different supply voltages and compared with simulations. The measured frequency sensitivity is 0.077 GHz per 10 mV at 15 GHz and matches with simulation. The simulated type A prescaler and the simulated three-stage prescaler have much higher sensitivity, 0.382 GHz per 10 mV at 15 GHz and 0.454 GHz per 10 mV at 15 GHz respectively.
3.2 A 60 GHz injection-locked inductorless divider-by-4 in 40 nm CMOS

Figure 3.11: Measurement setup with the 60 GHz transmitter. The prescaler oscillation frequency is derived by measuring the PLL divided output frequency.
Figure 3.12: Example of measured LR. The 60GHz QVCO frequency is swept and the prescaler’s oscillation frequency is observed. The locked condition is marked with a thicker line.

Figure 3.13: Free-running prescaler’s oscillation frequency tuned over the full scale of the PMOS load bank. Different settings of $V_{DAC_H}$ and $V_{DAC_L}$, coded with $DAC-H$ and $DAC-L$ in this measurement, give different tuning ranges.
3.2 A 60 GHz injection-locked inductorless divider-by-4 in 40 nm CMOS

Figure 3.14: Prescaler’s LR moved over frequency. The LR is larger with higher settings of the PMOS bank because of the more enhanced nonlinearity in the PMOS load bank itself.

Figure 3.15: Free-running oscillation frequency of the different prescaler types for changing supply voltage. The measurement result agrees with simulation (type B) and is compared to the simulation of the three-stage and the type A prescalers.
3.3 Conclusions

Inductor-less ILFDs are often used as mm-wave prescaler of mm-wave PLLs because they have a low power consumption, are compact and can be tuned over a wide frequency range. State of the art already offers such mm-wave inductor-less ILFDs [Hoshino07] [Decanis11]. However, these topologies appear to be sensitive to supply disturbances, a key performance parameter when the circuit is used within a complex system.

In this context, this Ph.D. work proposes an alternative topology, which is more robust against power-supply disturbances. It is a 60-15 GHz inductor-less prescaler in 40 nm low-power digital CMOS technology. It consists of a four-stage injection-locked ring oscillator with differential pairs as delay stages. The delay cell consists of a differential amplifier where the 60 GHz signal is injected through the tail current sources. Differently from [Hoshino07] and [Decanis11], the differential amplifiers have a hybrid load. This load consists of a differential binary-weight PMOS-triode resistive bank connected between the two differential output nodes, and two polysilicon resistors connecting the output nodes to the power-supply node. This prescaler has been designed as part of a 60 GHz PLL. This PLL has been integrated in a 60 GHz four-path phased-array receiver and in a 60 GHz four-path phased-array transmitter [Vidojkovic13a] [Vidojkovic13b].
Chapter 4

Conventional subharmonic injection locking

4.1 Introduction

Subharmonic injection locking is an appealing technique for frequency synthesis since it allows to synthesize a higher-frequency spectrally pure signal starting from a lower-frequency spectrally pure signal. In a typical realization, a high-frequency oscillator, running around frequency $f_0$, is locked to a subharmonic signal of frequency $f_0/n$, with $n$ an integer. The phase noise spectrum of the high-frequency oscillation follows the phase noise spectrum of the injected signal with a degradation factor of $20 \log_{10}(n)$ [Lee09].

The low-frequency signal can e.g. be provided by a low-frequency PLL. For certain frequency ranges and certain technologies, a frequency synthesizer that is subharmonically injection-locked to a lower-frequency PLL can perform equally to or even better than an equivalent higher-frequency PLL\footnote{This depends mainly on the technological limitations of the PLL spectral purity. Such limitations are usually due to the quality factor of the passives used for the frequency synthesis, such as the inductors and the varactors of the VCO.} [Chan08], [Musa11]. The phase noise spectrum of the injection-locked oscillator follows the phase noise spectrum of the subharmonic injected signal only at low offset frequencies. At higher offset frequencies, the noise floor of the injecting circuitry and of the rest of the circuit come into the picture [Chen08].

Another advantage of a high-frequency synthesizer locked to a low-frequency PLL is that it does not require high-frequency dividers\footnote{High-frequency dividers may still be required, though, for calibration or runtime control. This requirement can be overcome by enlarging the frequency range over which the high-frequency oscillator can be locked. This will be discussed and solved in Chapters 5 and 6.}. This is particularly appealing when the targeted oscillation frequency becomes more and more comparable to the cut-off frequency of the technology. Some examples of applications can be mm-wave transceivers.
(e.g., 60 GHz communication, 79 GHz car radar, 90 GHz imagers) or integrated THz sensors.

Phased-array transceivers can benefit from a further advantage by adopting a subharmonic injection-locked LO. In such transceivers, there is typically a long distance between the PLL and the mixers of the various front-ends. The PLL output signal therefore needs to be distributed over these long distances. With subharmonic injection locking, the PLL operates at \( f_0/n \) instead of operating at \( f_0 \). Consequently, a signal at an \( n \) times lower frequency needs to be distributed, thus lowering the power consumption of the LO distribution. Furthermore, operating at a lower frequency implies that the LO distribution is less sensitive to the parasitic capacitances and/or inductances. Moreover, an LO distribution at a lower frequency can facilitate the realization of phase shifting in the LO path\(^3\).

A 60 GHz four-path phased array receiver has been realized in a 90 nm CMOS technology, with an LO system based on subharmonic injection locking. In this system, described in Section 4.2, the signal coming from a lower-frequency (12 GHz) QVCO is distributed to the four antenna paths, locking four 60 GHz QVCOs. The goal of this realization is to prove the feasibility of subharmonic injection locking in the context of phased-array transceivers.

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\(^3\)Phase shifting is needed by phase-array transceivers in order to steer the antenna radiation pattern.
4.2 A 60 GHz injection-locked local oscillator in 90 nm CMOS

4.2.1 System overview: 60 GHz four-path phased array receiver

A 60 GHz LO system based on subharmonic injection locking has been investigated, designed and integrated in a 60 GHz four-path phased array receiver in 90 nm CMOS [Raczkowski12]. A block diagram of the receiver is shown in Fig. 4.1. Each antenna path is provided with a 60 GHz SHIL-QVCO, which is locked to the common 12 GHz LO. The baseband and the phase shifters, described in [Raczkowski12], are out of the scope of this Ph.D. work. As depicted in Fig. 4.1 and in Fig. 4.3a, the 12 GHz LO consists of a 12 GHz QVCO, a 12 GHz polyphase filter (PPF) and a 12 GHz distribution (buffers and transmission lines). Thus, the 60 GHz SHIL-QVCO can be locked either to the on-chip 12 GHz or to an external 12 GHz signal\(^4\). The use of subharmonic injection locking allows for LO phase shifting at a lower frequency (12 GHz instead of 60 GHz). Moreover, all the 60 GHz circuitry can be confined in a small area close to the front-end, as suggested in the block diagram of Fig. 4.1 and shown in the micrograph of Fig. 4.2. This enhances the modularity of this design with respect to an eventual increase of number of antennas.

In addition to the receiver, a dedicated test structure has been realized in order to test the LO system separately. A block diagram is depicted in Fig. 4.3b. With respect to the receiver’s LO system (Fig. 4.3a), the test structure has only one 60 GHz SHIL-QVCO. A micrograph is shown in Fig. 4.4.

It is very important to design the test structure so that it works at the same conditions as the four-path receiver does. Since in the test structure only one antenna path is reproduced, single-ended MOM capacitors (of about 0.5 pF) have been added at each of the four output terminals of the 12 GHz quadrature buffer in order to emulate the parasitic capacitance of the other three antenna paths, as depicted in Fig. 4.3b.

Contributions of this Ph.D. work

For these two 90 nm chips, this Ph.D. has investigated, designed and measured the subharmonic (12 GHz) LO circuitry, focusing on the 12 GHz QVCO and the 12 GHz LO distribution. This Ph.D. has also contributed to the investigation of the 60 GHz SHIL-QVCO. A conference publication [Raczkowski12] has been partially derived from what is discussed in this section.

\(^4\)A differential 12 GHz signal can be injected into the chip and converted into quadrature format by the 12 GHz PPF.
Figure 4.1: System diagram of the 60 GHz four-path phased array receiver in 90 nm CMOS. All the 60 GHz circuits are located close to the front end. The 12 GHz LO signal (coming either from the on-chip 12 GHz QVCO or from the PPF) is distributed to each of the four front ends. The baseband and the phase shifters, described in [Raczkowski12], are out of the scope of this Ph.D. work.
4.2 A 60 GHz injection-locked local oscillator in 90 nm CMOS

Figure 4.2: Chip micrograph of the 60 GHz four-path phased array receiver in 90 nm CMOS. The whole 60 GHz circuitry is located close to the four front-ends.

Figure 4.3: System diagram of the LO circuit on: (a) the four-path phased array receiver; (b) the dedicated test structure, where some MOM capacitance has been added in order to emulate the parasitic capacitance of other three antenna paths. The 60 GHz SHIL-QVCO can lock to either the on-chip 12 GHz QVCO or to an external 12 GHz signal.
Figure 4.4: Chip micrograph of the LO test structure realized in 90 nm CMOS.
4.2.2 Circuit design

12 GHz QVCO

The 12 GHz QVCO developed in this subsection is an extension of a previously published VCO [Geis10] and consists of two LC VCOs coupled to each other in a quadrature fashion, as depicted in Fig. 4.5. Transistors \( M_{1a,b} \) provide the negative resistance to sustain the oscillation. The strength of the quadrature coupling - operated by transistors \( M_{2a,b} \) can be mitigated by the cascode current sources \( M_{3a,b} \). Transistors \( M_1, M_2 \) and \( M_3 \) have the same dimension: \( W/L = 180 \mu m / 80 \) nm.

The phase noise of the 12 GHz QVCO is an important parameter since it will dictate the phase noise of the 60 GHz SHIL-QVCO. From a system-level specification\(^5\), the phase noise of the 60 GHz SHIL-QVCO is required to be lower than \(-90\) dBc/Hz at 1 MHz offset from the carrier, implying for the 12 GHz QVCO a phase noise lower than \(-104\) dBc/Hz at 1 MHz offset. Thanks to an RC bias network, the gates of \( M_{1a,b} \) can be biased differently from the drain bias, allowing a reduction of phase noise and thus improving performance.

\[ \text{Figure 4.5: Circuit schematic of the 12 GHz QVCO.} \]

\(^5\)The system-level analysis is not mentioned in this text since it is out of scope.
12 GHz LO distribution

The 12 GHz LO distribution consists of an active part and a passive part, as depicted in Fig. 4.6. The passive part consists of inductors and variable capacitors. The inductor resonates at 12 GHz with the total capacitance. This *inductive peaking* allows to reduce the power consumption of the active part. The $Q$ factor of the inductors and the capacitors is low enough to allow for a wideband operation. The variable capacitors allow for frequency tuning to cope with PVT variations. The active part amplifies the 12 GHz signal coming either from the QVCO (bit $inputSel$ high) or from the PPF (bit $inputSel$ low). The active part consists of CMOS inverters. Without the inductive peaking, such a CMOS logic would have required an unacceptable power consumption for a 12 GHz operation in the 90 nm technology. More advanced nodes (e.g. 28 nm) may allow a 12 GHz operation without inductive peaking at an acceptable power consumption.

![Figure 4.6: Schematic of the 12 GHz distribution, consisting of an active part (colored red) and a passive part for inductive peaking (colored blue).](image)

60 GHz SHIL-QVCO

The 60 GHz SHIL-QVCO schematic is shown in figure 4.7. It consists of two VCOs coupled to each other through transistors $M_{2a,b}$. Transistors $M_{3a,b}$ provide negative resistance. The subharmonic 12 GHz signal is injected through transistors $M_{4a,b}$. An RLC notch filter is provided at the drain of these transistors, in order to attenuate the 12 GHz
spurs and only leave the fifth harmonic of the signal, which is the actual locking signal [Kuo10]. The current of the cross-coupled pair is partially delivered by the injection locking transistors and partially by the transistors that provide the series coupling between the two VCOs. In this way, power consumption is lowered thanks to the current reuse and thanks to the fact that the LC tank is not additionally loaded by the injection-locking transistors.

Figure 4.7: Circuit schematic of the 60 GHz SHIL-QVCO [Raczkowski12] (I VCO part only). The gates of the injecting transistors $M_{2a,b}$ are biased by the injecting 12 GHz circuit.
4.2.3 Measurement results

The measurement results presented here have been mainly obtained from the LO test structure (Fig. 4.4). This chip has been mounted on a dedicated printed circuit board (PCB), with all the low-frequency IO pads bonded with the PCB connections and the mm-wave IO pads (12 GHz and 60 GHz) left free for on-chip probing. The measurement setup for the LO test structure is depicted in Fig. 4.8. An external 12 GHz signal is injected into the chip. A list of the most important measurement equipment consists of:

- 60 GHz RF spectrum analyzer (Rohde&Schwarz FSU67GHz),
- 20 GHz signal generator (Rohde&Schwarz SMR 40),
- signal analyzer for phase-noise measurements (AGT 5052B).

![Figure 4.8: Measurement setup for the LO test structure.](image)

The 12 GHz QVCO consumes from 13 mW to 20 mW under a 1.0 V supply. The 60 GHz SHIL-QVCO consumes typically 32 mW (ranging from 25 to 90 mW) under a 1.2 V supply. The 1.2 V supply (>1.0 V) is needed to ensure the oscillation startup.

60 GHz SHIL-QVCO under lock

The typical LR is 250 MHz at 60 GHz, with a tuning range from 58 to 62 GHz. An example of the LR is shown in Fig. 4.9: the settings of the SHIL-QVCO have been kept fixed and the injected signal’s frequency has been swept. The locked condition is marked with a thicker line, ranging from 61.27 GHz to 61.52 GHz.

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Footnote: The complete measurement setup includes also a number of DC sources, a computer, cables and instrumentation amplifiers. Most of the equipment is remotely controlled with the industry-standard GPIB bus.
4.2 A 60 GHz injection-locked local oscillator in 90 nm CMOS

Figure 4.9: Oscillation frequency and amplitude of the 60 GHz SHIL-QVCO under 12 GHz injection. The locked condition is marked with a thicker line.

The 60 GHz SHIL-QVCO cannot lock to the fifth oscillation harmonic of the 12 GHz QVCO because of an unexpected frequency mismatch. Although the simulated tuning range of the 12 GHz QVCO is 10.4-14.4 GHz, the measured tuning range is from 8.4 GHz to 11.1 GHz. This is due to an erroneous modelling of the inductor. Since the SHIL-QVCO is centered at 60 GHz with a tuning range of ± 2 GHz, it is not possible to lock to the fifth harmonic of the 8.4-11.1 GHz oscillation range. However, with a very fine tuning and a very narrow LR, it has been possible to lock on the sixth harmonic, as shown in Fig. 4.10 (the traces show spurs and are noisy at offset frequencies lower than 10 kHz because of the DC supply). Such an even-harmonic lock is not robust on differential circuits and therefore cannot be considered for a proper system operation. However, in this context such a lock is interesting in order to observe the phase noise of the SHIL-QVCO under lock, which follows the 12 GHz QVCO phase noise with a factor of 15.6 dB, as expected.

Fig. 4.11 reports the phase noise of the SHIL-QVCO when locked to an external 12 GHz signal (the spurs due to the DC supply have been graphically removed). At low offset frequencies, the SHIL-QVCO phase noise follows the injected signal’s phase noise with a degrading factor of approximately 14 dB, in agreement with the harmonic ratio. However, the phase noise degradation factor reaches 26 dB at 1 MHz offset. This further degradation can be due to the noise added by the on-chip injecting circuitry. More specifically, there are three main noise contributions to the output phase noise [Chen08]:

- the injected-signal phase noise originating from by the 12 GHz QVCO, which con-
Conventional subharmonic injection locking

tributes at offset frequencies lower than the single-sideband LR:
• the noise coming from the injecting circuitry, which contributes at offset frequencies lower than the single-sideband LR;
• the noise of the rest of the SHIL-QVCO circuitry, which contributes at offset frequencies higher than the single-sideband LR.

As a result, if the 12 GHz external injected signal has a very low phase noise, the noise contribution of the 12 GHz injecting circuitry dominates and causes the 26 dB degradation. In other words, a sort of SHIL-QVCO noise floor appears. The reader is invited to read some considerations on such a phase-noise floor, in Chapter 5, Subsections 5.5.3 and 5.5.4.

Figure 4.10: Phase noise of the SHIL-QVCO when locked to the on-chip 12 GHz QVCO, which is unexpectedly running at 10 GHz instead of 12 GHz (the traces show spurs and are noisy at offset frequencies lower than 10 kHz because of the DC supply).

Trading off the locking range

The LR has been measured for different settings of the SHIL-QVCO and some trade-offs have been observed. Fig. 4.12 reports the LR for different settings of the tail current source $M_5$ of Fig. 4.7. For a lower tail current (lower setting $I_{bias}$), the LR is enlarged but the oscillation amplitude is reduced. A similar result is found in Fig. 4.13, where a stronger quadrature coupling (higher current in $M_6$ of Fig. 4.7) enhances the oscillation amplitude but reduces the LR. Fig. 4.14 shows the influence of the gate bias voltage of the
4.2 A 60 GHz injection-locked local oscillator in 90 nm CMOS

![Graph showing phase noise of SHIL-QVCO](image)

Figure 4.11: Phase noise of the SHIL-QVCO when locked to the external 12 GHz signal (the spurs due to the DC supply have been graphically removed).

Injecting transistors $M_{2a,b}$: there is an optimal voltage bias for the largest $LR$. This can be explained by the fact that, for such optimal bias, the generation of the fifth harmonic is enhanced.

All the observations mentioned above agree with the model of injection-locked LC oscillators where the $LR$ is related to the oscillation current $I_{osc}$ and the injected current $I_{inj}$ [Razavi04] (see Chapter 2, Section 2.2):

$$LR = \frac{\omega_0}{Q} \frac{I_{inj}}{I_{osc}} \frac{1}{\sqrt{1 - \left(\frac{I_{inj}}{I_{osc}}\right)^2}}, \quad (4.1)$$

where $\omega_0 = 1/\sqrt{LC}$ is the LC-tank self-resonance frequency and $Q$ is the LC-tank quality factor. If current $I_{osc}$ is increased (Fig. 4.12 and Fig. 4.13), the $LR$ is decreased and the oscillation amplitude is increased. If the $n$-th harmonic generation is enhanced (Fig. 4.14), current $I_{inj}$ is enhanced and the $LR$ is increased, but not significantly.

To sum up, the $LR$ can mostly be enlarged at the expense of the oscillation amplitude.

Fig. 4.15 reports two extreme cases: narrow $LR$ and large oscillation amplitude versus wide $LR$ and small oscillation amplitude. On one hand, a large $LR$ is preferable in order to avoid the loss of lock because of disturbances. On the other hand, a minimal oscillation amplitude assumes that the SHIL-QVCO operates in current-limited regime, which is typically the case for 60 GHz oscillators in this CMOS technology.
amplitude is required for a proper operation of the LO system.

Figure 4.12: LR for different bias settings of the tail current source ($I_{bias}$ in Fig. 4.7). The higher the current bias, the higher the oscillation amplitude but the narrower the locking range.
4.2 A 60 GHz injection-locked local oscillator in 90 nm CMOS

Figure 4.13: LR for different bias settings of quadrature-coupling ($I_{coup}$ in Fig. 4.7). The higher the current bias, the higher the oscillation amplitude but the narrower the locking range.

Figure 4.14: LR for different bias settings of injection (gate voltage bias of $M_{2a,b}$ in Fig. 4.7). The higher the voltage bias, the higher the oscillation amplitude. There is an optimum bias for the largest LR.
Figure 4.15: Trade off between LR and oscillation amplitude. The LR can be significantly enlarged but with a significant penalty in oscillation amplitude.
4.3 Conclusions

Subharmonic injection locking is an appealing technique of frequency synthesis, especially for phased-array antenna radios. It allows to synthesize a high-frequency spectrally pure LO signal starting from an n times lower-frequency spectrally pure signal. No high-frequency divider is needed. The LO signal, which has to be distributed to the various antenna paths, has a lower frequency, thus simplifying the LO distribution and lowering power consumption.

A 60 GHz four-path phased array receiver has been realized in 90 nm CMOS technology, with an LO system based on subharmonic injection locking. The signal coming from a lower-frequency (12 GHz) QVCO is distributed to the four antenna paths, thus locking four 60 GHz SHIL-QVCOs. For testing purposes, there is the possibility of locking the SHIL-QVCOs to an external 12 GHz signal. The 12 GHz distribution simply consists of CMOS inverters with inductive peaking to lower the power consumption. This receiver demonstrates the feasibility of subharmonic injection locking for mm-wave frequency synthesis and, as discussed in [Raczkowski12], the benefit for beamforming based on LO phase shifting. Together with this receiver, an LO test structure has been fabricated, to further investigate the subharmonic injection-locking technique.

The 60 GHz SHIL-QVCO consumes typically 32 mW (ranging from 25 to 90 mW) under a 1.2 V supply. The typical LR is 250 MHz at 60 GHz, with a tuning range from 58 to 62 GHz. The SHIL-QVCO phase noise follows the phase noise of the 12 GHz QVCO as expected. When an external 12 GHz signal is used instead of the on-chip 12 GHz QVCO, the SHIL-QVCO phase noise is further reduced and a noise floor of −110 dBc/Hz appears for offset frequencies higher than 2 MHz. This can be due to the noise floor of the injecting circuitry.

One of the main parameters of a SHIL-QVCO is the locking range (LR). It is defined as the frequency range over which the SHIL-QVCO can be locked. It is measured under fixed SHIL-QVCO settings and sweeping the frequency of the injected subharmonic signal. The experiments presented in this chapter show that the LR can be enlarged at the expenses of the oscillation amplitude. On one hand, a large LR is preferable in order to avoid the loss of lock because of disturbances. On the other hand, a minimal oscillation amplitude is required for a proper operation of the LO system and for a good carrier-to-noise ratio.

For a robust operation, the LR should be (relatively) large without compromising the oscillation amplitude. For this purpose, this Ph.D. work has investigated an alternative SHIL-QVCO design, which is described in Chapter 5.

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8In [Raczkowski12], the beamforming is based on a hybrid phase shifting operated partially at LO and partially at baseband.
Chapter 5

Subharmonic injection locking with wide locking range

5.1 Introduction

The locking range (LR) is an important design parameter for frequency synthesizers based on subharmonic injection locking. The LR of a subharmonically injection-locked oscillator (SHILO) is often narrow because the locking phenomenon relies on the generation of the $n$-th harmonic of the injected subharmonic signal (see Chapter 2, Section 2.2). Consequently, an accurate tuning of the SHILO is needed to match the narrow LR with the targeted frequency [Deng12]. Moreover, a narrow LR makes the system sensitive to disturbances that may suddenly bring the SHILO out of lock. A wider LR is preferred to simplify the SHILO control and to improve robustness against disturbances. The LR can be enlarged by injecting a stronger subharmonic signal, leading to higher power consumptions. A moderate, but still significant improvement comes from enhancing the $n$-th harmonic generation [Chen08]. The LR of LC-tank SHILOs can be enlarged by lowering the $Q$ factor of the LC tank, as done in [Chan08]. This, however, also results into an increased power consumption for a given oscillation amplitude.

For this Ph.D. work, the SHILO design is further complicated because the 60 GHz LO frequency is required to be in quadrature format (I/Q) as the LO signal is used in a direct-conversion architecture. For this task, the SHILO topology has been chosen to be a 60 GHz subharmonically injection-locked QVCO (SHIL-QVCO), as depicted in Fig. 5.1. The design of such a SHIL-QVCO is complicated because two different locking mechanisms must be considered:

- the injection locking between the two oscillators forming the QVCO [Mirzaei07],
- the injection locking of the SHIL-QVCO on the $n$-th harmonic of the reference signal [Chan08] [Razavi04] [Chen08].
Figure 5.1: Function of the 60 GHz SHIL-QVCO: generates a 60 GHz I/Q signal, with an acceptable I/Q phase accuracy, locked to a 60/n GHz subharmonic signal that is available in I/Q format.

This Ph.D. proposes to realize a 60 GHz SHIL-QVCO with a large LR using coupled-LC tanks. Section 5.2 explains the use of such coupled-LC tanks, compares these with single-LC-tank approaches, and derives design guidelines. Section 5.3 describes calibration techniques when using the coupled-LC tanks. The coupled-LC approach is demonstrated in two SHIL-QVCO realizations. The first realization of a SHIL-QVCO with a wide locking range (SHIL-QVCO\textsubscript{W1}) is described in section 5.4, while the second realization of a SHIL-QVCO with a wide locking range (SHIL-QVCO\textsubscript{W2}) is described in section 5.5. Finally, section 5.6 draws conclusions. The results described in this chapter have resulted into two conference publications [Mangraviti12], [Mangraviti13b].
5.2 Coupled-LC tanks for wide locking range

This section explains how coupled-LC tanks can fulfill the locking condition of an SHILO over a large frequency range. This is very beneficial for mm-wave SHILOs, which typically have narrow LRs.

5.2.1 Principle of large LR with coupled-LC tanks

Coupled-LC tanks can achieve a large LR if they are designed such that the phase of the tank impedance is close to zero over a large frequency range. More specifically, referring to the ILO model of Fig. 2.2 and to the locking condition expressed by (2.8), a large LR can be achieved by making $|Z_{\text{tank}}|$ smaller than $\alpha_{\text{lock}}$ over a large frequency range. Fig. 5.2 depicts a simplified model of a coupled-LC-tank ILO, where the resonant tank consists of the two resonators, $L_1C_1$ and $L_2C_2$, coupled to each other with a coupling factor $k$. The impedance of such a resonant tank, $Z_{\text{tank}}(\omega)$, is depicted in Fig. 5.3. It has been derived by simulating the circuit of Fig. 5.3a, for different values of $k$, with the parameters reported in Table 5.1. For a particular value of $k$, the phase $\angle Z_{\text{tank}}(\omega)$ forms a flat region around $0^\circ$. In the following, we will refer to such a flat region as phase plateau. Thanks to this phase plateau, a large LR can be achieved since (2.8) holds over a large frequency range.

The phase plateau in $Z_{\text{tank}}(\omega)$ results from the combination of one zero at $\omega = 0$, one pair of complex conjugate zeros and two pairs of complex conjugate poles. In order to approximately estimate the frequencies of the poles and zeros of $Z_{\text{tank}}(\omega)$, $Q$ is approximated to be infinite. This is a crude approximation because $Q$ has a value around 10 in the application described in the following. However, this approximation simplifies calculations and is expected not to drastically vary the frequencies of poles and zeros. With this premise, it is found that (see Appendix A.1):

$$Z_{\text{tank}}(\omega) = \frac{j\omega L_1 (1 - \omega^2 / \omega_z^2)}{(1 - \omega^2 / \omega_{p1}^2)(1 - \omega^2 / \omega_{p2}^2)},$$

(5.1)
Figure 5.3: Coupled-LC tank: (a) schematic; (b) phase and (c) magnitude of $Z_{\text{tank}}(\omega)$ for different values of $k$, derived by a simulation of the circuit in (a).

where

$$
\omega_z := \frac{\gamma \omega_1}{\sqrt{1-k^2}},
$$

$$
\omega_{p1} := \omega_1 \sqrt{\frac{\gamma}{1+k}}, \quad \omega_{p2} := \omega_1 \sqrt{\frac{\gamma}{1-k}},
$$

$$
k \leq 1, \quad \gamma := \omega_2/\omega_1,
$$

$$
\omega_1 := 1/\sqrt{L_1C_1}, \quad \omega_2 := 1/\sqrt{L_2C_2}.
$$

(5.2)
Table 5.1: LC values of the simulated coupled-LC tank.

<table>
<thead>
<tr>
<th>$L_1$</th>
<th>$L_2$</th>
<th>$Q_{L_1}$</th>
<th>$Q_{L_2}$</th>
<th>$k$</th>
</tr>
</thead>
<tbody>
<tr>
<td>50 pF</td>
<td>100 pF</td>
<td>10</td>
<td>10</td>
<td>0.2 (phase plateau)</td>
</tr>
<tr>
<td>$C_1$</td>
<td>$C_2$</td>
<td>$Q_{C_1}$</td>
<td>$Q_{C_2}$</td>
<td></td>
</tr>
<tr>
<td>140 fF</td>
<td>76 fF</td>
<td>10</td>
<td>10</td>
<td></td>
</tr>
</tbody>
</table>

Notice that $\omega_{p_1} < \omega_z < \omega_{p_2}$ and that the coupling factor $k$ influences the position of both the poles and the zeros. Also notice that $Z_{\text{tank}}(\omega)$ is purely imaginary in (5.1) because $Q$ was assumed to be infinite.

These poles and zeros can be positioned so that $Z_{\text{tank}}(\omega)$ exhibits a phase plateau at $0^\circ$, as shown in Fig. 5.4. Considering the phase asymptotic behavior and assuming that zeros and poles have the same $Q$ factor\(^1\), it is found that a phase plateau at $0^\circ$ requires approximately (see Appendix A.2):

$$k = \frac{10^{1/Q} - 1}{10^{1/Q} + 1}$$  \hspace{1cm} (5.3)

and

$$\gamma = \sqrt{1 - k^2} \iff \frac{L_1C_1}{L_2C_2} = 1 - k^2.$$  \hspace{1cm} (5.4)

The value of $k$ is established at design time, while condition (5.4) can be fulfilled by tuning $C_1$ and $C_2$, as proposed in section 5.3.

### 5.2.2 Design of the coupled-LC tank

Design guidelines can be derived for a coupled-LC tank, operating at a targeted frequency $\omega_{\text{target}}$. The phase plateau is always centered at $\omega_z$ (Fig. 5.4). Given that we size the two resonators $L_1C_1$ and $L_2C_2$ according to (5.4), (5.2) simplifies towards

$$\omega_{\text{target}} = \omega_z = \omega_1.$$  \hspace{1cm} (5.5)

From the considerations above the following design strategy is proposed:

1. choose $\omega_{\text{target}}$;
2. enforce $L_1C_1 = 1/\omega_1^2 = 1/\omega_{\text{target}}^2$;
3. choose $k$ starting from the approximate value in (5.3);

\(^1\)Now that we focus on the phase, a finite $Q$ has to be considered since it strongly affects the phase behavior of poles and zeros. The $Q$ factor of a complex-conjugate pair of poles/zeros is defined as $\frac{\xi}{2}$, with $\xi$ the damping factor. The $Q$ factor of poles and zeros is assumed to be the same because poles and zeros share the same inductors ($L_1$ and $L_2$) and the same capacitors ($C_1$ and $C_2$). The $Q$ factor will then be affected by the same parasitic conductance of capacitors and the same parasitic resistance of inductors.
Subharmonic injection locking with wide locking range

Figure 5.4: Phase contributions of poles and zeros to $\angle Z_{tank}(\omega)$. The combination of the poles and zeros (bottom graph) makes $\angle Z_{tank}(\omega)$ exhibit a phase plateau at $0^\circ$.

4. size $L_2C_2$ according to (5.4), given $L_1C_1$ and $k$;
5. fine tune $k$ and the other parameters during the design flow.

Note that all the derivations above come from approximate calculations. Therefore, more design iterations may be required, especially for mm-wave IC design where parasitics (e.g. parasitics from interconnections and transistors) play an important role.

A 60 GHz design example can be made, as illustrated in the following, resulting in the values of Table 5.1. For 60 GHz applications, transformer inductors are typically in the order of 50-100 pH. Assuming that the active MOS core is connected to the primary resonator $L_1C_1$, $C_1$ should be sized large enough to include the MOS parasitic capacitances. Because of this, we can choose a low inductor value, $L_1=50$ pH. Taking the output signal from the secondary resonator $L_2C_2$ (as done in the two SHIL-QVCOs described
5.2 Coupled-LC tanks for wide locking range

It is convenient to have $L_2 > L_1$ in order to boost the voltage transfer function. Here we can choose $L_2 = 2 \times L_1 = 100 \text{pH}$. A $Q = 10$ is assumed for both inductors and (variable) capacitors, as it is a typical value at mm-wave frequencies in CMOS, thus resulting in LC tanks with $Q = 5$. The design steps proposed above then become:

1. $\omega_{\text{target}} = 2\pi \times 60 \text{GHz}$;
2. $L_1 C_1 = 1/\omega_{\text{target}}^2 \rightarrow C_1 \simeq 140 \text{fF}$;
3. (5.3) with $Q = 5 \rightarrow k \simeq 0.23$;
4. (5.4) $\rightarrow C_2 \simeq 74 \text{fF}$;
5. after fine-tuning design iterations, we obtain $k = 0.2$ and $C_2 = 76 \text{fF}$.

Fig. 5.3b shows that the parameters obtained above result in a phase plateau which covers approximately a frequency range from 58 to 62 GHz.

The width of the phase plateau is mainly fixed by the $Q$ factor. More specifically, this width is linked to the ratio $\omega_2/\omega_1$, which must be set equal to $\sqrt{1-k^2}$, according to (5.4). The coupling factor $k$ is fixed by (5.3) for a given $Q$.

5.2.3 Comparison with single-resonance approaches

Three kinds of resonators are compared for mm-wave LC-tank SHILOs: single-LC tank [Musa11], [Raczkowski12], single-LC tank with lowered $Q$ [Chan08] and coupled-LC tank [Mangraviti12] [Li14]. These three approaches are qualitatively compared in Fig. 5.5 by observing the phase and the magnitude of $Z_{\text{tank}}(\omega)$. The phase $\angle Z_{\text{tank}}(\omega)$ influences the LR (2.8), while the magnitude $|Z_{\text{tank}}(\omega)|$ influences the oscillation amplitude (assuming the oscillator operates in current-limited regime). The oscillation amplitude is important for two reasons:

- Phase noise: given the noise floor of the LO buffers, a minimum SNR is needed to avoid degradation of phase noise.
- LO signal driving mixers: the conversion mixers require a minimum LO oscillation swing.

This comparison is meant to qualitatively illustrate advantages and disadvantages of the three approaches, in terms of LR and oscillation amplitude.

The three resonators have been chosen as follows. The single-LC tank (1-LC in Fig. 5.5) and the two resonators $L_1 C_1$ and $L_2 C_2$ of the coupled-LC tank (2-LC in Fig. 5.5) have been modelled with the same $Q$ factor. More specifically, inductors have $Q=10$ and capacitors have $Q=10$, thus LC tanks with $Q=5$. Such $Q$ factors are generally dictated by the particular CMOS technology and by the operating frequency. The coupled-LC tank is sized according to Table 5.1 and the single-LC tank is sized with $L=L_1$ and $C=C_2$. The single-LC tank with lowered $Q$ factor (low $Q$ in Fig. 5.5) has $L=L_1$ and $C=C_2$, and an additional parallel conductance has been added so that the impedance phase allows the same LR as the coupled-LC tank does (see Fig. 5.5a).
Subharmonic injection locking with wide locking range

Figure 5.5: Comparison of $Z_{\text{tank}}(\omega)$, according to (a) phase and (b) magnitude of a single-LC tank (1-LC), a single-LC tank with low $Q$ (low-Q) and a coupled-LC tank (2-LC). Here $\alpha_{\text{lock}}$ is set to 7°.

The single-LC approach offers a narrow LR but a large oscillation amplitude. Therefore, a single-LC tank without $Q$ degradation is generally preferable in terms of oscillation amplitude but offers narrower LR and thus requires frequency tracking [Deng12]. A single-LC tank with $Q$ degradation offers a larger LR [Chan08], but it is expected to give rise to a small oscillation amplitude. On the other hand, a coupled-LC tank offers a large LR with a moderate penalty in oscillation amplitude.

To sum up, with respect to single-LC tanks, the coupled-LC tank offers a better trade-off between LR and oscillation amplitude. This is paid with more complexity in the design. Because of this, design guidelines are given in Subsection 5.2.2.
5.2 Coupled-LC tanks for wide locking range

5.2.4 State-of-the-art of coupled-LC tanks for mm-wave LOs

Multi-order LC tanks are already used in the state of the art for mm-wave frequency synthesis in CMOS, but for purposes differing from subharmonic injection locking. This subsection is meant to show that coupled-LC tanks are already known for mm-wave CMOS applications. The novelty of this Ph.D. work is the use of coupled-LC tanks to enlarge the LR of subharmonically injection-locked mm-wave oscillators by shaping the phase of $Z_{tank}(\omega)$.

Some examples of the state of the art follow, which describe mm-wave CMOS VCOs using coupled-LC tanks (not for subharmonic injection locking). References [Lee07] and [Li09] use different inductors in order to locally resonate with the parasitic capacitance of varactors and cross-coupled MOS transistors, thus improving efficiency, phase noise performance and tuning range. Reference [Yin13] describes a transformer-based dual-band VCO where coupled-LC tanks allow for an ultra-wide frequency tuning range. Reference [Decanis11] describes a low-noise two-stage ring oscillator where coupled-LC tanks are used to couple the two delay stages to accurately determine the oscillation frequency. The $90^\circ$ phase shift needed by each delay stage is provided by $Z_{21}$ of the coupled-LC tanks. In contrast with [Decanis11], in the coupled-LC injection-locking technique described in this Ph.D. work, the free-running oscillation frequency cannot be accurately determined: if no injection is applied then the oscillator can oscillate at any of the frequencies at which $\angle Z_{tank}(\omega) = 0$. This indetermination of the free-running frequency leads to a large LR.

Higher-order LC tanks are also used, differently from this Ph.D. work, to enhance the LR of injection-locked frequency dividers. Reference [Takatsu10] improves the injection efficiency of the injecting transistor. More specifically, a pair of inductors is inserted between the output nodes of the ILFD and the source/drain of the injecting transistor. This forms a multi-order LC oscillator where the effective parasitic capacitance across the LC tank circuit is reduced, thus enhancing the LR because the LR is inversely proportional to the parasitic capacitance in such an ILFD. Reference [Yin12] improves the injection efficiency by creating a frequency-dependent phase shift for the total injected current.
5.3 Calibration of a coupled-LC tank

The coupled-LC tank needs to be calibrated such that the impedance $Z_{\text{tank}}(\omega)$ exhibits a phase plateau at $0^\circ$. This means that equations (5.3) and (5.4) must be satisfied. The condition of equation (5.3) can be accomplished with a proper design of the coupling factor $k$ of the coupled-LC-tank transformer. The condition of equation (5.4) can be reached by calibrating the ratio $C_2/C_1$.

![Figure 5.6: Phase and magnitude of the coupled-LC $Z_{\text{tank}}$ for different $C_2/C_1$ ratios](image)

Figure 5.6: Phase and magnitude of the coupled-LC $Z_{\text{tank}}$ for different $C_2/C_1$ ratios ($k=0.2$, $L_1=50\ \text{pH}$, $L_2=2L_1$, $C_1=140\ \text{fF}$, $C_2=69$, 76 and 83 fF). Markers $\omega_{FR1}$, $\omega_{FR2}$ and $\omega_{FR3}$ mark the free-running oscillation points for the three capacitor ratios. When the phase plateau is at $0^\circ$, $|Z_{\text{tank}}|$ is minimum at the free-running oscillation frequency ($\omega_{FR2}$).

![Figure 5.7: Coupled LC-tank seen as a two-port.](image)

Figure 5.7: Coupled LC-tank seen as a two-port.

The proposed calibration procedure relies on the fact that $|Z_{\text{tank}}(\omega)|$ experiences a local minimum between two resonant peaks and, when the phase plateau is set to $0^\circ$, the free-running oscillation occurs at this local minimum. Fig. 5.6 shows $Z_{\text{tank}}(\omega)$ (phase and magnitude) for the given $k$ and for different $C_2/C_1$ ratios. The circuit parameters
used for simulation are the ones in Table 5.1 with $k=0.2$ and $C_2=69$, 76 and 83 fF. The phase plateau is located above or below $0^\circ$ as $C_2/C_1$ is higher or lower than the desired ratio expressed in (5.4).

If no injection is applied, the injection-locked oscillator operates in free-running mode. The oscillation will then occur at the frequency at which $Z_{\text{tank}}(\omega) = 0$, defined as the free-running frequency $\omega_{\text{FR}}$. Fig. 5.6 shows that $\omega_{\text{FR}}$ becomes lower or higher as $C_2/C_1$ is lower or higher than the desired ratio. Moreover, $|Z_{\text{tank}}(\omega = \omega_{\text{FR}})|$ experiences a relative minimum if $C_2/C_1$ is equal to the desired ratio. Thus $C_2/C_1$ can be calibrated by detecting this relative minimum. Notice that, if the coupling factor $k$ is too low, the two resonant peaks cannot be distinguished from each other and hence this calibration procedure cannot be performed.

A first calibration method is to detect the relative minimum of $|Z_{\text{tank}}(\omega = \omega_{\text{FR}})|$ when sweeping ratio $C_2/C_1$. This minimum corresponds to the relative minimum of the free-running oscillation amplitude, $V_{\text{osc}}$ in Fig. 5.2 and Fig. 5.7, assuming that the output voltage $V_{\text{osc}}$ is proportional to $|Z_{\text{tank}}|$. This condition is fulfilled in current-limited regimes. The voltage-limited regimes are not considered since it would require an unacceptable power consumption for the targeted frequency with the current CMOS technology. The detection of this relative minimum can be implemented through a simple envelope detector.

A second calibration method is to calibrate $C_2/C_1$ by observing the amplitude of the coupled-LC secondary voltage, $V_2$ in Fig. 5.7. In the current-limited regime, $|V_2|$ is proportional to the coupled-LC transimpedance $|Z_{21}|$. Fig. 5.8 shows a simulation of $Z_{11}(\omega) \equiv Z_{\text{TANK}}(\omega)$ and $Z_{21}(\omega)$, where the resonators have $Q = 5$ (similarly to what has been done for the simulation in Fig. 5.3) and $L_2/L_1 = 2$ to boost the voltage transfer. Notice that $|Z_{21}(\omega)|$ has only one peak and thus no local minimum (see the approximate...
Subharmonic injection locking with wide locking range

Figure 5.9: Impedance magnitudes $|Z_{11}(\omega = \omega_{FR})|$ (dashed line) and $|Z_{21}(\omega = \omega_{FR})|$ (continuous line), and free-running oscillation frequency $f_{FR}$ for different ratios $C_2/C_1$. The circuit parameters used for the simulation are the same as used for Fig. 5.6, with $C_2$ swept from 69 to 83 fF. The calibration of $C_2/C_1$ can be done detecting either the relative minimum of $|Z_{11}(\omega = \omega_{FR})|$ or the steep change of $|Z_{21}(\omega = \omega_{FR})|$ or the frequency step of $f_{FR}$. Notice that $C_2/C_1 \approx 1/2$ because $L_2/L_1 = 2$.

analysis of poles and zeros of $Z_{21}(\omega)$ in Appendix 5.1). However, $|Z_{21}(\omega = \omega_{FR})|$ exhibits an interesting behavior when $C_2/C_1$ is swept, as shown in Fig. 5.9: the local minimum of $|Z_{11}(\omega_{FR})|$ corresponds to a steep change of $|Z_{21}(\omega_{FR})|$. As a result, $C_2/C_1$ can be calibrated by detecting a steep change in $|Z_{21}(\omega_{FR})|$.

A third calibration method is to calibrate $C_2/C_1$ by observing the free-running oscillation frequency $\omega_{FR}$ while sweeping $C_2/C_1$. As observable in Fig. 5.9, $\omega_{FR}$ has a steep change in correspondence with the relative minimum of $|Z_{11}(\omega_{FR})|$.

After looking for procedures to set the phase plateau at 0°, a next question is how to shift such a 0° phase plateau over frequency. This is important for an LO system, which must be able to generate different frequencies required by the communication standard\(^2\). Further, it is useful to shift the LR over frequency in order to compensate possible process variations.

The LR is shifted over frequency by changing $C_1$ and then recalibrating $C_2/C_1$. This phase plateau’s frequency shift is simulated and shown in Fig. 5.10. Thanks to the large LR, there is no need for a fine resolution in this frequency shift. What is finally important is to calibrate the ratio $C_2/C_1$. Therefore, $C_1$ can be designed as a low-resolution variable capacitor and $C_2$ as a higher-resolution variable capacitor.

Having ways to shift the phase plateau over frequency and to set such a phase plateau at 0°, we come to the following calibration procedure, targeting a certain operating fre-

\(^2\)For instance, the WiGig standard for 60 GHz requires LO frequencies from 58 GHz to 65 GHz.
5.3 Calibration of a coupled-LC tank

Figure 5.10: Phase plateau for different values of $C_1$ for constant $C_2/C_1$. The phase plateau, and consequently the LR, can be moved over frequency.

frequency range:

**step 1**: tune $C_1$ such that the phase plateau covers the targeted frequency range;

**step 2**: tune $C_2$ such that $C_2/C_1$ satisfies (5.4).

A frequency measurement may be required in **step 1**, but it is meant for coarse tuning. The fine tuning is done at **step 2** and requires no frequency measurement. This can be done by sweeping $C_2$ and detecting the relative minimum of $V_{osc}$ (**first calibration method**), or the steep change in $V_2$ (**second calibration method**), or the steep change in the free-running oscillation frequency (**third calibration method**). The **first** and the **second** calibration methods are based mainly on a relative mm-wave amplitude measurement and therefore can be considered simpler than frequency-based calibrations [Deng12].

The calibration can be performed off-line since the ILO is expected to stay locked during runtime thanks to the large LR. Therefore, no frequency control or any other calibration is needed during runtime. This is an advantage with respect to systems with narrow LR where a runtime frequency control is required [Lee08]. The calibration proposed here can be further simplified and made more robust by means of lock detection [Man-gravity13b] as illustrated in Chapter 6.
5.4 First realization: a 52-66 GHz SHIL-QVCO with 10 GHz locking range in 40 nm CMOS

The coupled-LC approach described in section 5.2 has been realized in two 60 GHz SHIL-QVCOs. The first SHIL-QVCO, described in this section, is denoted\(^3\) as SHIL-QVCO\(_{W1}\). The second one is described in section 5.5 and is denoted as SHIL-QVCO\(_{W2}\).

5.4.1 System overview

The 60 GHz SHIL-QVCO described here (SHIL-QVCO\(_{W1}\)) has been integrated in a 60 GHz transceiver [Vidojkovic12], realized in a 40 nm low-power digital CMOS technology. The block diagram of the whole LO system is reported in Fig. 5.11. A quadrature 20 GHz signal (\(\text{Inj } I+\), \(\text{Inj } I-\), \(\text{Inj } Q+\) and \(\text{Inj } Q-\), with DC bias voltage \(\text{V}_{\text{gate inj}}\)) is injected into SHIL-QVCO\(_{W1}\). This signal is derived from a single-ended external 20 GHz signal, using an on-chip balun followed by a polyphase filter (PPF) and buffers. The output of SHIL-QVCO\(_{W1}\) is buffered to the RF front-ends. Fig. 5.12 shows a micrograph of the LO system.

![Figure 5.11: Block diagram of the LO system in which SHIL-QVCO\(_{W1}\) operates.](image)

Contributions of this Ph.D. work

For this 40 nm chip, this Ph.D. work has contributed with:

- formulation and study of the coupled-resonance approach for wide LR;
- study and evaluation of such an approach applied to the SHIL-QVCO;
- complete design and simulation of the SHIL-QVCO;
- top-level coordination of the design of the LO system;
- measurement and characterization of the LO system.

A conference publication [Mangraviti12] has been derived from what is discussed in this section.

\(^3\)The letter \(W\) in acronyms SHIL-QVCO\(_{W1}\) and SHIL-QVCO\(_{W2}\) stays for wide LR.
5.4 First realization: a 52-66 GHz SHIL-QVCO with 10 GHz locking range in 40 nm CMOS

**Figure 5.12:** Chip photo of the LO system in which SHIL-QVCO operates. The low-band SHIL-QVCO has not been measured.

### 5.4.2 Circuit design

The circuit design of the two most important subblocks, the 20 GHz PPF and the 60 GHz SHIL-QVCO, is described next.

**20 GHz PPF**

The **PPF** consists of two RC stages, as drawn in Fig. 5.13. Such a **PPF** circuit provides output quadrature signals, $V_I$ and $V_Q$, whose amplitude mismatch depends on the frequency, and the phase difference is constantly 90° over the whole frequency band [Galal00]. The more RC stages are used (each stage is centered at a different frequency), the smaller the amplitude mismatch is. In this design, two stages are chosen, centered at 16 GHz ($R=100 \Omega$ and $C=100 \text{fF}$) and at 26 GHz ($R=100 \Omega$ and $C=61 \text{fF}$) respectively. The **PPF** simulated output (Fig. 5.14) shows a perfect quadrature phase over the whole operating frequency range, with an amplitude mismatch within 3% (corresponding to ~30 dB). Hereby it is assumed that there is no mismatch among corresponding components in the schematic of Fig. 5.13. An analysis of amplitude and phase imbalance in the presence of component mismatches is outside of the scope of this Ph.D. work.
Figure 5.13: Schematic of the 2-stage RC PPF. The first stage is centered at 16 GHz ($R_2=100 \Omega$, $C_2=100 \text{ fF}$) and the second stage at 26 GHz ($R_1=100 \Omega$, $C_1=61 \text{ fF}$).
5.4 First realization: a 52-66 GHz SHIL-QVCO with 10 GHz locking range in 40 nm CMOS

Figure 5.14: Output of the 20 GHz PPF, obtained from a small-signal circuit simulation: (a) phases and (b) magnitudes. The phases differ always by 90° from each other. The magnitudes, normalized to the PPF differential input, show a mismatch of maximum 3% around 20 GHz.
Subharmonic injection locking with wide locking range

60 GHz SHIL-QVCO$_{W1}$

The SHIL-QVCO$_{W1}$ circuit schematic is shown in Fig. 5.15. It consists of two differential oscillators coupled to each other via transistors $M_3$ and $M_4$, in order to enforce quadrature operation [Mirzaei07]. Each differential oscillator consists of a coupled-LC tank and a MOS active core. More specifically, the primary LC tank ($L_1C_1$) is connected to the negative conductance (cross-coupled MOS transistors $M_1$ and $M_2$) while the secondary LC tank ($L_2C_2$) is connected to the output buffers.

Varactors $C_1$ and $C_2$ allow for tuning and calibration. Varactor $C_1$ has been designed for low resolution (2-bit), while varactor $C_2$ has a high resolution (2-bit coarse tuning, 4-bit fine tuning and an analog varactor). All the capacitive banks consist of switched differential MOS varactors having a gate length of 80 nm (the widths are reported in Table 5.2).

The core of the coupled resonator is the transformer (Fig. 5.16). A coupling factor $k \approx 0.2$ is requested for the phase plateau (5.3). The ratio $L_2/L_1$ has been chosen to be larger than one (here $L_1 \simeq 50 \text{ pH}$ and $L_2 \simeq 93 \text{ pH}$) in order to boost the voltage swing fed to the output buffers. Ground walls surround the transformer in order to confine the electromagnetic field locally, thus lowering the influence of the adjacent circuits on the transformer’s performance. Despite the simplified drawing of Fig. 5.16, these ground walls do not form a closed loop, otherwise they would degrade the transformer’s $Q$ factor.

The design of SHIL-QVCO$_{W1}$ starts from the transformer. Then, the varactors and the active core are dimensioned such that (5.4) holds over the whole targeted frequency range. After some iterations, the design flow has resulted into the sizes reported in Table 5.2.

Similarly to [Raczkowski12], in the MOS active core the injecting transistors $M_5$ and
First realization: a $52-66$ GHz SHIL-QVCO with $10$ GHz locking range in $40$ nm CMOS

\[
P_{2}+ P_{2} - P_{1}+ P_{1} - kL_{1} L_{2}
\]

\[
\text{tap}_1, \text{tap}_2 \quad \text{(different metal layers)}
\]

Figure 5.16: Transformer used in the coupled-LC tank of SHIL-QVCO$_{W1}$, with $k \approx 0.22$, $L_1 \approx 50\mu H$ and $L_2 \approx 95\mu H$. $L_2/L_1$ has been chosen to be larger than one in order to boost the voltage signal fed to the output buffers.

Table 5.2: Sizes of SHIL-QVCO$_{W1}$.

<table>
<thead>
<tr>
<th>Component</th>
<th>$L_1$</th>
<th>$L_2$</th>
<th>$k$</th>
<th>$Q_1$</th>
<th>$Q_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>50 pH</td>
<td>93 pH</td>
<td>0.22</td>
<td>8</td>
<td>7</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Component</th>
<th>$M_1,2$, $M_{3,4}$, $M_{5,6}$, $M_{7,8}$, $M_{9,10}$</th>
</tr>
</thead>
<tbody>
<tr>
<td>W/L ((\mu m / nm))</td>
<td>26 / 50, 26 / 50, 26 / 50, 600 / 60, 20 / 80</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Component</th>
<th>$C_1$, $C_2$, $C_2$, $C_2$</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>(2-bit), (2-bit), (4-bit), (analog)</td>
</tr>
</tbody>
</table>

| W/L of the least significant bit (\(\mu m / nm\)) | 18 / 80, 9 / 80, 2.4 / 80, 4.8 / 80 |
|minimum - maximum (fF) | 21 - 41, 10.5 - 21, 15 - 29, 2 - 4 |

$M_6$ do not load the LC tank but are connected in series with the cross-coupled pair $M_{1,2}$. This reduces the parasitic capacitance loading the LC tank and potentially improves the system efficiency thanks to the current reuse.

The DC current of the active cores comes from the tail current sources $M_7$ and $M_8$. 
whose currents are mirrored as depicted in Fig. 5.15. The MOS branches for the quadra-
ture coupling ($M_3$ and $M_4$) are biased by $M_7$ and the MOS branches for the subharmonic
injection ($M_5$ and $M_6$) are biased by $M_8$. The tail current sources $M_7$ and $M_8$ are sized
and driven so that they draw a DC current of about 6 mA and 12 mA respectively.

Notice that, from the DC point of view, the active cores of SHIL-QVCO present
three MOS devices in a stack. This leads to problems with the voltage headroom as
$M_7$ and $M_8$ cannot operate in saturation. Moreover, the oscillation swing is eventually
reduced since the negative resistance (i.e. the cross-coupled MOS pair) has its source
terminals on top of a stack of two MOS devices. Such issues are solved in another design,
which uses another topology for the active core and is described in Section 5.5.
5.4 First realization: a 52-66 GHz SHIL-QVCO with 10 GHz locking range in 40 nm CMOS

5.4.3 I/Q phase accuracy

The SHIL-QVCO must provide a 60 GHz I/Q signal with good I/Q phase accuracy. The I/Q phase accuracy of SHIL-QVCO is influenced by two concurrent mechanisms: the active quadrature coupling between the two differential oscillators (via $M_3$ and $M_4$) and the quadrature multi-phase subharmonic injection (Fig. 5.17). The former mechanism can lead to I/Q phase errors if mismatches are present between the two differential oscillators [Mirzaei07]. The quadrature multi-phase injection can lead to SHIL-QVCO I/Q phase errors if the injected signal itself is affected by an I/Q phase error $\Delta \phi_{IQ_{in}}$. It has to be noticed that a phase error $\Delta \phi_{IQ_{in}}$ in the 20 GHz injected signal would correspond to a 60 GHz phase error $\Delta \phi_{IQ_{out}} = 3 \times \Delta \phi_{IQ_{in}}$ if no phase correction is applied by the SHIL-QVCO.

![Figure 5.17: Input and output I/Q phases of the 60 GHz SHIL-QVCO. The undesired phase errors are represented by $\Delta \phi_{IQ_{in}}$ and $\Delta \phi_{IQ_{out}}$.](image)

I/Q output phase error

Simulations show that an input phase error $\Delta \phi_{IQ_{in}}$ is partially corrected by the SHIL-QVCO itself. Fig. 5.18 shows that $\Delta \phi_{IQ_{out}} < 3 \Delta \phi_{IQ_{in}}$. This demonstrates that the coupling of $M_3$ and $M_4$ fights the phase imbalance, thus enhancing the robustness against input phase errors at 20 GHz.

The I/Q phase error may degrade at the LR edges. Fig. 5.19 shows the simulated $\Delta \phi_{IQ_{out}}$ over the whole LR for different values of $\Delta \phi_{IQ_{in}}$. However, $\Delta \phi_{IQ_{out}}$ always remains below $3 \Delta \phi_{IQ_{in}}$, validating the benefit of the active coupling between the two differential oscillators. Notice that the phase responses of Fig. 5.19 are not symmetric with respect to $\Delta \phi_{IQ_{in}}$; in other words, $\Delta \phi_{IQ_{out}}(\Delta \phi_{IQ_{in}}) \neq \Delta \phi_{IQ_{out}}(-\Delta \phi_{IQ_{in}})$. This can be due to the fact that the phase plateau is not exactly at 0°.

Fig. 5.18 and Fig. 5.19 show the simulated $\Delta \phi_{IQ_{out}}$ under locked condition. The SHIL-QVCO has been first calibrated in free-running state as suggested in the calibration procedures of Section 5.3. Secondly, the LR has been evaluated with transient simulations. Finally, periodic-steady-state simulations have been used to evaluate $\Delta \phi_{IQ_{out}}$
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Figure 5.18: Simulated average $\Delta \phi_{IQ_{out}}$ (at 60 GHz) for different values of $\Delta \phi_{IQ_{in}}$ ($\Delta \phi_{IQ_{in}}$ at 20 GHz $\rightarrow 3 \Delta \phi_{IQ_{in}}$ at 60 GHz). Clearly, $\Delta \phi_{IQ_{out}} < 3 \Delta \phi_{IQ_{in}}$ thanks to the active coupling of $M_3$ and $M_4$. For each $\Delta \phi_{IQ_{in}}$, $\Delta \phi_{IQ_{out}}$ is averaged over the whole LR (62.3-68.3 GHz). The voltage swing at the gates of $M_5$ and $M_6$ is 0.4 Vpp.

Figure 5.19: Simulated $\Delta \phi_{IQ_{out}}$ (around 60 GHz) over the whole LR, for different values of $\Delta \phi_{IQ_{in}}$ (at 20 GHz).

over the different locked frequencies\(^4\). No transistor mismatch has been taken into account since here the scope is only the evaluation of the output phase error $\Delta \phi_{IQ_{out}}$ in presence of an input phase error $\Delta \phi_{IQ_{in}}$ on the injected subharmonic signal.

\(^4\)The simulation procedure for a coupled-LC-tank SHIL-QVCO is described in Section 5.5.
5.4 First realization: a 52-66 GHz SHIL-QVCO with 10 GHz locking range in 40 nm CMOS

**LR versus I/Q input phase**

This Ph.D. work prefers an I/Q subharmonic injection over a simpler differential subharmonic injection for two reasons:

- multiphase injection enlarges the LR of an injection-locked oscillator [Mirzaei08];
- a SHIL-QVCO with differential injection suffers from a large I/Q error [Musa11].

On the other hand, the I/Q phase of the injected signal must correspond to $90^\circ$ at 60 GHz for an optimal injection locking. Considering a subharmonic frequency of $60/n$ GHz, the I/Q input phase must be:

\[
90^\circ \text{ at } 60 \text{ GHz} \equiv \frac{90^\circ}{n} + \frac{k}{n} 360^\circ \text{ at } \frac{60}{n} \text{ GHz}, \tag{5.6}
\]

with $k$ an integer. This implies a desired I/Q input phase of $30^\circ$, $150^\circ$ or $-90^\circ$ for a 20 GHz injection. Fig. 5.20 shows indeed that the simulated LR of SHIL-QVCO$_{W1}$ is maximal for such desired input phases and is minimal for the opposite phases. In the realization described here, the 20 GHz PPF provides an I/Q phase of $-90^\circ$ at 20 GHz, which matches with a phase of $90^\circ$ at 60 GHz.

Regarding this phase matching, it should be considered that a QVCO can potentially run in either one of two modes: $+90^\circ$ and $-90^\circ$ [Mirzaei07]. Typically, one mode has more gain and/or is more stable than the other mode. In the QVCO topology of Fig. 5.15, the delay of $M_3$ and $M_4$ facilitates one mode instead of the other. However, to overcome a possible mode ambiguity, it is advisable to foresee the possibility of inverting the sign of the subharmonic input phase so that the injected signal matches the QVCO mode. This can be done by swapping the "I" signal with the "Q" signal in the subharmonic circuit.
Subharmonic injection locking with wide locking range

Figure 5.20: Simulated LR versus the IQ input phase. The LR is maximum for input phases which correspond to $90^\circ$ at 60 GHz (i.e. $-90^\circ$, $30^\circ$ and $150^\circ$ at 20 GHz). The LR is minimum for input phases which correspond to $-90^\circ$ at 60 GHz (i.e. $-150^\circ$, $-30^\circ$ and $90^\circ$ at 20 GHz). The voltage swing at the gates of $M_5$ and $M_6$ is 0.6 Vpp.
5.4 First realization: a 52-66 GHz SHIL-QVCO with 10 GHz locking range in 40 nm CMOS

5.4.4 Measurement results

The 60 GHz transceiver, in which SHIL-QVCO<sub>W1</sub> is integrated, has been mounted on a dedicated printed circuit board (PCB), with all the low-frequency IO pads bonded with the PCB connections and three mm-wave IO pads for on-chip probing, as indicated in Fig. 5.21.

![Micrograph of the 60 GHz transceiver](image)

Figure 5.21: Micrograph of the 60 GHz transceiver where SHIL-QVCO<sub>W1</sub> is integrated. The mm-wave pads for the measurement probes are indicated.

The measurement setup is depicted in Fig. 5.22. An external 20 GHz signal is injected into the chip. The SHIL-QVCO has been measured through the transmitter’s 60 GHz output and the receiver’s baseband output. The most important measurement instruments are:

- 60 GHz RF spectrum analyzer (Rohde&Schwarz FSU67GHz),
- 20 GHz signal generator (Rohde&Schwarz SMR 40),
- 67 GHz signal generator (Agilent E 8257D),
- time-domain oscilloscope with 4 channels (Tektronix TDS 6124C),

The complete measurement setup includes also DC sources, a computer, cables and instrumentation amplifiers. Most of the equipment is remotely controlled with the industry-standard GPIB bus.
Subharmonic injection locking with wide locking range

Figure 5.22: Measurement setup where the SHIL-QVCO \( W \) has been characterized using the transmitter’s 60 GHz output and the receiver’s baseband output.

- signal source analyzer for phase-noise measurements (AGT 5052B),
- arbitrary waveform generator (Tektronix AWG 7102).

Calibration

Since no amplitude detection has been foreseen at the coupled-LC tank’s primary resonator, the SHIL-QVCO can only be calibrated by observing its output oscillation, i.e. the oscillation at the coupled-LC tank’s secondary (see the second calibration method described in Section 5.3). This output oscillation has been observed through the transmitter and receiver front-end output pads\(^6\). The top plot in Fig. 5.23 shows the free-running output amplitude and oscillation frequency for a fixed \( C_1 \) and different (fine-tuning) settings of \( C_2 \). The free-running amplitude and frequency have a steep change in the proximity of \( C_2 \) setting ‘8’. The bottom plot of Fig. 5.23 shows that the LR is wide for this \( C_2 \) setting. It can be observed that the free-running amplitude drops dramatically at \( C_2 \) setting ‘8’, but it is restored under injection, as reported in Fig. 5.24. It can be further observed from Fig. 5.23 that the LR is also wide for other settings of \( C_2 \). This is due to the fact that in this QVCO design the oscillation swing is relatively small. This issue is solved in a further SHIL-QVCO design, described in Section 5.5.

\(^6\) The 60 GHz output RF pad of the transmitter and the baseband output pads of the receiver.
5.4 First realization: a 52-66 GHz SHIL-QVCO with 10 GHz locking range in 40 nm CMOS

Figure 5.23: Measured free-running output amplitude and frequency (top plot) and LR (bottom plot) for a fixed $C_1$ and different (fine-tuning) settings of $C_2$. Calibration step 2 can be performed by measuring the steep change either of the free-running output amplitude or of the free-running oscillation frequency.

**Locking range**

The sensitivity of the LR to the single-ended amplitude of the 20 GHz injected signal is shown in Fig. 5.25. An amplitude of about 250 mV is sufficient to achieve a wide LR.

As explained in section 5.3, the LR can be moved over frequency by changing $C_1$ and then recalibrating $C_2$ accordingly. The LR of SHIL-QVCO$_{W1}$ is shown in Fig. 5.52 for different $C_1$ settings. Thanks to this tunability, operation is possible over all the four 60 GHz communication channels [Vidojkovic12]. This tunability is also beneficial for accommodating the operation against process variations.
Figure 5.24: Output power of SHIL-QVCO\textsubscript{W1} under free-running condition and under injection locking.

Figure 5.25: Measured LR versus injected 20 GHz signal peak-peak swing (single-ended). An input swing of 450 mVpp is sufficient to obtain a wide LR. The reported signal amplitude is the voltage swing at \(M_{5,6}\) gates. This has been estimated from the power injected into the 20 GHz input of the chip.

Figure 5.26: Measured LR for different \(C_1\) settings.
5.4 First realization: a 52-66 GHz SHIL-QVCO with 10 GHz locking range in 40 nm CMOS

The image rejection ratio of the RF front-ends has been considered as figure of merit for the SHIL-QVCO I/Q phase accuracy. The measured image rejection ratio is 30 dB for the receiver and 22 dB for the transmitter [Vidojkovic12], which would correspond to phase errors of $3^\circ$ and $8^\circ$ respectively\(^7\).

Simulations and measurements show that only part of the whole LR is reliable for operation: the SHIL-QVCO output voltage amplitude typically degrades at the LR edges. Fig. 5.27 shows the baseband output of the receiver front-end over the whole LR. It can be seen that, over 10 GHz of LR, a frequency range of about 6 GHz can be used for operation. Of course, the mixer plays an important role in this: the smaller the required LO input for the mixer is, the closer one can operate to the LR edges. However, it can be argued that, for a robust operation, it is preferable to have a narrower LR but with a large and uniform oscillation amplitude over the whole LR\(^8\). This argument is the subject under investigation on the second realization of a SHIL-QVCO with a wide locking range (SHIL-QVCO\(_W\)) described in Section 5.5.

Figure 5.27: Measured receiver baseband output power over the LR. Only part of the whole LR can be used for the front-end operation.

---

\(^7\)Assuming no amplitude imbalance.

\(^8\)The oscillation amplitude is important for phase noise and for a good operation of mixers, as mentioned in Subsection 5.2.3.
Phase noise

The SHIL-QVCO phase noise is shown in Fig. 5.28. Under injection locking, the phase noise is mainly dictated by the signal injected via the 20 GHz buffers into the SHIL-QVCO. At 1 MHz offset from the carrier, the measured phase noise is better than $-96$ dBc/Hz over the whole 60 GHz band [Vidojkovic12]. Because of the multiplication factor between 20 GHz and 60 GHz, the SHIL-QVCO phase noise should be degraded with respect to the injected external signal phase noise by a factor of $20\log_{10}(3) \approx 9.5$ dB.

However, Fig. 5.28 shows a phase noise degradation of 23 dB at 1 MHz offset, much higher than the expected 9.5 dB. Reference [Chen08] explains such a rise in the phase noise with the noise floor of the circuits involved in the subharmonic injection and in the $n$-th harmonic generation. The same phenomenon has been observed on the SHIL-QVCO discussed in Chapter 4 and on the measured and simulated SHIL-QVCO presented in Section 5.5.
5.4 First realization: a 52-66 GHz SHIL-QVCO with 10 GHz locking range in 40 nm CMOS

5.4.5 Comparison with the state of the art

A comparison to other published solutions is shown in Table 5.3. The work of [Musa10] and [Chan08] describe stand-alone SHIL-QVCOs, while [Okada11] and [Chan10] describe their respective integration in a system. All the SHIL-QVCOs reported in this comparison operate at 60 GHz and are locked to a 20 GHz input signal. For a system comparison, the power consumption of the whole LO systems (60 GHz SHIL-QVCOs together with the 20 GHz circuitry and the 60 GHz buffers) is considered per antenna path. The power consumption of the proposed LO system is comparable to the other solutions, but a wider LR (> 9 GHz) is achieved and the calibration can be simplified with respect to frequency control. Moreover, the wide LR can be moved over frequency, covering a broader frequency range (52 to 66 GHz).
Table 5.3: Comparison with other published solutions

<table>
<thead>
<tr>
<th></th>
<th>This Ph.D. work [Mangraviti12]</th>
<th>[Musa10] [Musa11]</th>
<th>[Chan08]</th>
</tr>
</thead>
<tbody>
<tr>
<td>LC-tank topology</td>
<td>Coupled-LC tank</td>
<td>Single-LC tank</td>
<td>Low-Q-LC tank</td>
</tr>
<tr>
<td>Technology</td>
<td>40nm LP CMOS</td>
<td>65nm CMOS</td>
<td>90nm CMOS</td>
</tr>
<tr>
<td>LR [GHz]</td>
<td>&gt; 9</td>
<td>0.3</td>
<td>8</td>
</tr>
<tr>
<td>Overall LR [GHz]</td>
<td>52-66</td>
<td>58-65.4</td>
<td>Not tunable, 56.5-64.5</td>
</tr>
<tr>
<td>Calibration</td>
<td>Mainly based on relative power measurement; in principle not needed during runtime</td>
<td>Frequency tracking; maybe needed during runtime because of narrow LR</td>
<td>In principle not needed, but LR cannot be moved over frequency</td>
</tr>
<tr>
<td>Pdc [mW]</td>
<td>37</td>
<td>14.4-52.8</td>
<td>9.6</td>
</tr>
<tr>
<td>(only SHIL-QVCO)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VDD (V)</td>
<td>1.1</td>
<td>1.2</td>
<td>1</td>
</tr>
<tr>
<td>System integrating the SHIL-QVCO</td>
<td>[Vidojkovic12]: 1-antenna TX-RX with 1×SHIL-QVCO</td>
<td>[Okada11]: 1-antenna TX-RX with 2×SHIL-QVCO</td>
<td>[Chan10]: 4-antenna TX with 4×SHIL-QVCO</td>
</tr>
<tr>
<td>Pdc when integrated in the system [mW]</td>
<td>SHIL-QVCO: 37</td>
<td>2×SHIL-QVCO: 2×14.9</td>
<td>4×(SHIL-QVCO + Active 20GHz PPF + buffers): 4×60</td>
</tr>
<tr>
<td></td>
<td>1st LO buffer: 9</td>
<td>2×LO buffers: 2×10</td>
<td></td>
</tr>
<tr>
<td></td>
<td>RX LO buffer: 14</td>
<td>20GHz PLL: 66</td>
<td></td>
</tr>
<tr>
<td></td>
<td>TX LO buffer: 12</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>Bias control: 5</td>
<td></td>
<td></td>
</tr>
<tr>
<td></td>
<td>20GHz buffer: 35</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Pdc of 20GHz and 60GHz LO generation per antenna path [mW]</td>
<td>112 / 2 = 56</td>
<td>115.8 / 2 = 57.9</td>
<td>60</td>
</tr>
<tr>
<td></td>
<td></td>
<td>(PLL included)</td>
<td></td>
</tr>
</tbody>
</table>
5.5 Second realization: a 55-63 GHz SHIL-QVCO with different injected frequencies in 40 nm CMOS

The oscillator previously discussed, SHIL-QVCO\textsubscript{W1}, achieves a very large LR but the oscillation amplitude is small for a large part of the LR. For a robust operation, it is preferable to have a narrower LR with a large and uniform oscillation amplitude over the complete LR\textsuperscript{9}. This is one of the main motivations of the following SHIL-QVCO design, denoted as SHIL-QVCO\textsubscript{W2}. The improvements with respect to SHIL-QVCO\textsubscript{W1} are that:

- the SHIL-QVCO can lock to different subharmonic frequencies, namely 60/n GHz with n=3, 5, 7 and 9;
- the LR, although narrower than SHIL-QVCO\textsubscript{W1}, is still large (larger than 2 GHz for an injected frequency of 20 GHz and larger than 0.8 GHz for an injected frequency of 7 GHz) and offers a large and uniform oscillation amplitude over the whole LR;
- an envelope detector facilitates the SHIL-QVCO calibration;
- a simple lock detector is included to ease the calibration (discussed in chapter 6).

5.5.1 System overview

The system consists mainly of five subblocks (see block diagram of Fig. 5.29):

- a 60 GHz SHIL-QVCO,
- an envelope detector,
- a lock detector based on passive mixers (discussed in chapter 6),
- a 60 GHz downconverting mixer,
- a subharmonic I/Q chain of CMOS inverters and a buffer, operating at 60 GHz/n, with n an odd integer.

The technology used is 40 nm general-purpose digital CMOS. A chip micrograph is shown in Fig. 5.30.

Contributions of this Ph.D. work

This Ph.D. work has contributed with the design and the characterization of the whole chip corresponding to Fig. 5.29:

- investigation and design of a SHIL-QVCO with the coupled-LC-tank approach for large LR and with a uniform oscillation amplitude over the whole LR,
- design of an envelope detector for calibration,
- design of a lock detector (discussed in chapter 6),
- design of the subharmonic I/Q injecting chain,

\textsuperscript{9} The oscillation amplitude is important for phase noise and for a good operation of mixers, as mentioned in Subsection 5.2.3.
• design of the quadrature downconversion (to check the I/Q phase accuracy at an intermediate frequency),
• finalization of the chip design,
• simulation of the subblocks and the whole system,
• measurement and characterization of the whole system.

A conference publication [Mangraviti13b] has been derived from this work.
Figure 5.30: Micrograph of the 40 nm chip which integrates SHIL-QVCO$_{W2}$. 
5.5.2 Circuit design

60 GHz SHIL-QVCO\textsubscript{W2}

The 60 GHz SHIL-QVCO\textsubscript{W2} (see Fig. 5.31) consists of two differential LC-tank oscillators coupled to each other through transconductors \(M_3, 4\). The voltage headroom of the active core is less problematic than for the SHIL-QVCO\textsubscript{W1} design (described in Section 5.4 and depicted in Fig. 5.15). Further, the use of PMOS devices\textsuperscript{10} allows to connect the source terminals of the cross-coupled MOS pair directly to ground, thus enhancing the oscillation swing.

Coupled resonators \((L_1C_1 - L_2C_2)\) are used to achieve a large LR (section 5.2). The output signal is taken from the secondary resonator \((L_2C_2)\). A coupling factor \(k\) of 0.2 has been chosen, according to equation (5.3), as required for a large LR. In order to boost the output voltage swing, \(L_2=103\) p\(\Omega\) has been chosen to be larger than \(L_1=75\) p\(\Omega\). The transformer layout is drawn in Fig. 5.32, where the secondary winding is larger than the primary winding to allow \(L_2 > L_1\). The spacing between the two windings is large enough in order to obtain a low \(k\). The simulated transformer \(Q\) factor is around 13.5 at 60 GHz. Similarly to the transformer drawn in Fig. 5.16, ground walls are used to confine

\textsuperscript{10}The SHIL-QVCO\textsubscript{W2} described here has been designed to be realized in 40 nm general-purpose CMOS, while the SHIL-QVCO\textsubscript{W1} described in Section 5.4 has been designed for 40 nm low-power CMOS. PMOS transistors are much faster in the general-purpose flavour than in the low-power flavour and therefore can be used as part of the active core.
5.5 Second realization: a 55-63 GHz SHIL-QVCO with different injected frequencies in 40 nm CMOS

the EM field locally, thus lowering the influence of the adjacent circuits on the transformer’s performance. The cross-coupled pairs $M_{1,2}$ provide the negative conductance necessary for the oscillation. The subharmonic signal is injected into both differential oscillators through cascodes $M_{6,7}$ and $M_{6,8}$. The cascode topology is chosen to emphasize the $n$-th harmonic of the injected signal.

Similarly to the design strategy of SHIL-QVCO$_{W1}$, the design of SHIL-QVCO$_{W2}$ starts from the transformer. Then, the varactors and the active core are dimensioned such that (5.4) holds over the whole targeted frequency range. Differently from SHIL-QVCO$_{W1}$, the LR has now been traded off in favor of a more uniform oscillation amplitude over the whole LR. This has been obtained, with reference to equation (2.6), by enhancing $\frac{|I_{osc}|}{|I_{in}|}$ and thus lowering $\alpha_{lock}$. After some iterations, these considerations have resulted into the sizes reported in Table 5.4.

The SHIL-QVCO needs to be calibrated to allow for a large LR. Firstly, $C_1$ is chosen for the desired coarse value of the output frequency. Secondly, $C_2$ has to be tuned to obtain a particular ratio $C_2/C_1$. This can be done by sweeping $C_2$ and measuring the relative minimum of the free-running oscillation amplitude, as explained in Section 5.4. Differently from Section 5.4, an envelope detector is now used to monitor the amplitude of the oscillation at the primary resonator $(L_1C_1)$. This detector provides a DC output proportional to the oscillation amplitude. The setting of $C_2$, which gives a peak in the envelope response, implies a large LR as experimentally verified in Section 5.5.4.

The main design modifications of SHIL-QVCO$_{W2}$ with respect to SHIL-QVCO$_{W1}$ are summarized as:

- PMOS devices are used in the signal path and used as current generators.
The cross-coupled MOS pair of SHIL-QVCOW2 has the source terminals directly grounded while the cross-coupled MOS pair of SHIL-QVCOW1 is source degenerated. Therefore, SHIL-QVCOW2 offers higher oscillation voltage swing than SHIL-QVCOW1 does, implying also higher $|I_{osc}|$ and consequently narrower LR with respect to SHIL-QVCOW1.

The signal MOS devices in SHIL-QVCOW2 ($M_{3,4}$ and $M_{5,6}$ in Fig. 5.31) operate as common-source amplifiers while the signal MOS devices in SHIL-QVCOW1 ($M_{3,4}$ and $M_{5,6}$ in Fig. 5.15) operate in differential pairs. This enlarges the voltage headroom in SHIL-QVCOW2 with respect to SHIL-QVCOW1.
5.5 Second realization: a 55-63 GHz SHIL-QVCO
with different injected frequencies in 40 nm CMOS

Envelope detector

The envelope detector monitors the output amplitude of the SHIL-QVCO. The input is connected to the primary side of the SHIL-QVCO's LC tank. The detector's DC output follows the oscillation amplitude: higher oscillation amplitude causes lower DC output.

![Schematic of the envelope detector](image)

Figure 5.33: Schematic of the envelope detector.

The core circuit of the envelope detector is shown in Fig. 5.33. The circuit is biased to carry a current of about 0.2 mA. The key point is that the DC operating point of this circuit is strongly affected by the oscillation amplitude present at its inputs (in+ and in-). PMOS and NMOS transistors are biased separately (biasP and biasN), providing an additional degree of freedom. In this design no particular bias control loop has been foreseen. To keep symmetry between the two oscillators constituting the SHIL-QVCO, one envelope detector is connected to the in-phase oscillator and another envelope detector is connected to the quadrature-phase oscillator. The DC outputs of these two envelope detectors are then combined (short circuited) obtaining the cancellation of the second harmonic of the 60 GHz oscillation coming from the in-phase and the quadrature-phase.
oscillators. The DC output is compared with the output of a reference detector without input (see Fig. 5.33). The simulated transfer characteristic of the envelope detector is shown in Fig. 5.34. The (single-ended) SHIL-QVCO\textsuperscript{W2} amplitude is expected to be between 100 and 200 mV. Over such a range, the envelope detector’s response is fairly linear.
Subharmonic injecting chain

The subharmonic injecting chain distributes and injects a subharmonic signal of frequency $60/n$ GHz into the 60 GHz SHIL-QVCO. Additionally, it converts the single-ended $60/n$ GHz input signal into a $60/n$ GHz differential quadrature signal. Only odd integers $n$ can be used since the circuits are differential.

![Subharmonic injecting chain schematic](image)

Figure 5.35: Schematic of the subharmonic injecting chain.

The schematic of the subharmonic injection chain is drawn in Fig. 5.35. An external $60/n$ GHz signal is converted from single-ended to differential by an on-chip balun. This differential signal is buffered by two pseudo-differential lines ($I_{SH}$ and $Q_{SH}$) consisting of cascades of CMOS inverters. Line $Q_{SH}$ is delayed with respect to line $I_{SH}$ by a variable capacitive load. In this way, the necessary delay is obtained, which corresponds to the desired phase shift at the targeted frequency. The variable capacitive load consists of two binary-weight capacitors (4-bit) (denoted as $varC_{SH}$ in Fig. 5.35) whose differential capacitance ranges from 7 fF to 16 fF. The resulting signals ($I_{SH}^+, I_{SH}^-, Q_{SH}^+, Q_{SH}^-$)
are then buffered and injected into the SHIL-QVCO. Multiplexers MUX1 can be used to swap the differential input of line $Q_{SH}$, hence obtaining the inversion of the output quadrature phase. Multiplexers MUX2 are used to keep the symmetry between line $I_{SH}$ and line $Q_{SH}$.

In this design no particular control loop has been foreseen for the variable capacitive load. One possible implementation can use a mixer and a successive-approximation-register loop at the SHIL-QVCO output. The mixing of the 60 GHz in-phase output with the quadrature-phase counterpart only results in a DC component if the two signals are not 90° phase shifted. Such a DC component can be minimized by a successive-approximation-register operating on the variable capacitive loads of the subharmonic injecting chain.

As mentioned in subsection 5.4.3, for an optimal injection-locking efficiency, the phase difference between $I_{SH}$ and $Q_{SH}$ should match the I/Q phase of the SHIL-QVCO, which is 90° at 60 GHz. Therefore, the variable capacitive load is tuned such that:

$$\angle I_{SH} - \angle Q_{SH} = 90^\circ \text{ at } 60 \text{ GHz} \equiv \frac{90^\circ}{n} + \frac{k \times 360^\circ}{n} \text{ at } 60 \text{ GHz}, \quad (5.7)$$

with $k$ an integer. From (5.7) the optimal injection phases are derived for $n = 3, 5, 7$ and 9, as reported in Table 5.5. Fig. 5.36 shows the simulated I/Q output phase of the subharmonic delay line under injection of $60/n$ GHz, with $n = 3, 5, 7$ and 9. An optimal injection phase can be targeted for any of the reported $n$.

Table 5.5: Optimal $60/n$ GHz-injection phases corresponding to $90^\circ$ at 60 GHz.

<table>
<thead>
<tr>
<th>$n$</th>
<th>$30^\circ$</th>
<th>$150^\circ$</th>
<th>$270^\circ$</th>
</tr>
</thead>
<tbody>
<tr>
<td>$n=3$</td>
<td>$30^\circ$</td>
<td>$150^\circ$</td>
<td>$270^\circ$</td>
</tr>
<tr>
<td>$n=5$</td>
<td>$18^\circ$</td>
<td>$90^\circ$</td>
<td>$162^\circ$</td>
</tr>
<tr>
<td>$n=7$</td>
<td>$13^\circ$</td>
<td>$64^\circ$</td>
<td>$116^\circ$</td>
</tr>
<tr>
<td>$n=9$</td>
<td>$10^\circ$</td>
<td>$50^\circ$</td>
<td>$90^\circ$</td>
</tr>
</tbody>
</table>

---

11. Differential-pair buffers are used because of the legacy of a previous design. Cross-coupled capacitive feedback is used to neutralize the differential amplifier and to minimize the input Miller capacitance, thus minimizing the capacitive load seen by the CMOS inverters.

12. The inversion of the differential input of line $Q_{SH}$ corresponds to adding 180° to the phase delay of line $Q_{SH}$ with respect to line $I_{SH}$. If $\angle I_{SH} - \angle Q_{SH} = 90^\circ$ at 60 GHz without the input swap, with the input swap $\angle I_{SH} - \angle Q_{SH} = -90^\circ$ at 60 GHz. This can be useful for test purposes.

13. The simulation used is a periodic steady state analysis. Layout parasitics are taken into account.
Figure 5.36: Output I/Q phase of the subharmonic delay line for different delay settings (horizontal axis), under injection of $60/n$ GHz, with $n = 3, 5, 7$ and $9$. The injection phases (dashed lines) of $150^\circ$ ($n=3$), $162^\circ$ ($n=5$), $167^\circ$ ($n=7$) and $170^\circ$ ($n=9$) are optimal since these correspond to $90^\circ$ at $60$ GHz.
5.5.3 Simulation of injection locking

The injection-locking operation of SHIL-QVCO\(_{W2}\) has been simulated, with test benches resembling the one illustrated in Fig. 5.37. SHIL-QVCO\(_{W2}\) consists of the following blocks: two differential VCOs (VCO-I and VCO-Q) coupled to each other, VCO bias circuits, an envelope detector and lumped parasitics\(^\text{14}\). The subharmonic signal,

\(^\text{14}\)These lumped RC parasitics are estimated after simulating SHIL-QVCO\(_{W2}\) with layout parasitic extracted circuits.
5.5 Second realization: a 55-63 GHz SHIL-QVCO with different injected frequencies in 40 nm CMOS

which is injected through the gates of transistors $M_{5,6}$, is generated by ideal sinusoidal voltage sources ($SH-I$ and $SH-Q$).

**Calibration and injection locking**

The determination of the LR is done in two steps: a calibration under free-running condition and a frequency sweep under injection locking.

The first simulation step is meant to calibrate the SHIL-QVCO, as explained in Section 5.3. No injection is applied, thus letting the SHIL-QVCO run freely. The bias settings are kept fixed and the digital varactor $C_2$ is swept through different settings. A transient simulation is run for each setting of $C_2$. After skipping the transient (typically a couple of nanoseconds), the envelope detector’s output and the oscillation frequency are recorded.

A typical result of this first simulation step is shown in Fig. 5.38. The digital setting of $C_2$ is chosen such that it gives the maximum envelope detector’s output. Section 5.3 explained that this ensures a large LR and, under free-running condition, a steep change in oscillation frequency, as shown in Fig. 5.38.

The second simulation step is meant to evaluate the width of the LR. One keeps the setting of $C_2$ from the previous simulation step, and applies the subharmonic injection signal is applied. The subharmonic frequency is swept. For each value of subharmonic frequency, the SHIL-QVCO’s oscillation frequency is recorded after removing the initial transient (typically 5 ns).

A typical result of this second-step simulation is shown in Fig. 5.39, where a 20 GHz injection signal is applied. The SHIL-QVCO frequency is locked over the range from

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15The oscillation frequency is calculated as (the average of) the inverse of the oscillation zero-crossing periods.
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Figure 5.39: Simulation result of a LR evaluation, operated by sweeping the subharmonic injected frequency.

60 GHz to 62.7 GHz to the third harmonic of the injected frequency. Outside of this LR, the SHIL-QVCO oscillation frequency does not follow the \( n \)-th harmonic of the injected frequency.

**Phase noise**

The SHIL-QVCO\( _{W2} \) phase noise and the phase noise of the subharmonic injected signal have been computed from simulations both in free-running mode and under injection locking. Referring to the test bench of Fig. 5.37, the SHIL-QVCO phase noise has been computed on the differential signal probed between nodes \( I_3^+ \) and \( I_3^- \), while the subharmonic signal’s phase noise has been computed on the differential signal between nodes \( \text{Inj}_I^+ \) and \( \text{Inj}_I^- \). The goal of these simulations is to show the effect of subharmonic injection locking on the SHIL-QVCO phase noise. An exhaustive study on phase noise under injection locking is out of the scope of this Ph.D. work.

The simulated phase noise of free-running SHIL-QVCO\( _{W2} \) is shown in Fig. 5.40. The free-running oscillator has been first simulated with a harmonic-balance analysis\(^16\) and then with a harmonic-balance-noise analysis. The phase noise follows the typical frequency behaviour of a free-running oscillator: at low offset frequencies (<1 MHz) it decays by 30 dB/decade and for higher offset frequencies (>1 MHz) by 20 dB/decade.

A noise summary has been derived from simulations, as reported in Fig. 5.41. For low offset frequencies, the main noise contributors belong to bias circuits: (referring to Fig. 5.37) the bias circuits of nodes \( V_{bias} \) and \( V_{gate, cp} \) of \( \text{VCO-I} \), the bias circuit of node \( V_{gate, cp} \) of \( \text{VCO-Q} \) and the Flicker noise of current source \( M_0 \) of \( \text{VCO-I} \). For higher off-

\(^{16}\)Harmonic balance analysis for autonomous oscillators. Harmonic balance, which is a frequency-domain analysis, has been preferred to the time-domain periodic-steady-state analysis since it handles better the S-parameter models of passive components and interconnections.
5.5 Second realization: a 55-63 GHz SHIL-QVCO with different injected frequencies in 40 nm CMOS

Figure 5.40: Phase noise of free-running SHIL-QVCO\textsubscript{W2}.

set frequencies, the main contributors are the drain-current and the gate-resistance noise of transistors $M_{1,2}$ of VCO-I and VCO-Q. Other minor contributions - neglected in this context - come from the Flicker of bias circuits for low offset frequencies, and from the drain-current noise of devices of the VCO active cores for high offset frequencies. This noise summary will be compared with the noise summary obtained under injection locking in the following of this subsection. Although free running and injection locking share most noise contributors, the noise contributions are much lower in the case of injection locking.
Figure 5.41: Summary of the main noise contributors to the free-running SHIL-QVCO phase noise.
5.5 Second realization: a 55-63 GHz SHIL-QVCO with different injected frequencies in 40 nm CMOS

The phase noise of SHIL-QVCO, when injection-locked to a 20 GHz signal, has been simulated. The 20 GHz signal is sinusoidal and applied to nodes Inj I+, Inj I−, Inj Q+ and Inj Q− (Fig. 5.37). A white noise floor has been added to the ideal 20 GHz signal\textsuperscript{17}. Fig. 5.42 shows the results of three cases with different noise floors: −111 dBc/Hz (Fig. 5.42a), −131 dBc/Hz (Fig. 5.42b) and −166 dBc/Hz (Fig. 5.42c). In the first case (Fig. 5.42a), the SHIL-QVCO phase noise follows the 20 GHz signal phase noise with a factor of 9.7 dB, which is very close to the expected \(20\log_{10}(60/20)\) ≃ 9.5 dB. In the second case (Fig. 5.42b) the 20 GHz signal phase noise is 20 dB lower and a phase noise ratio higher than 9.5 dB appears at low offset frequencies (< 100 kHz). In the third case (Fig. 5.42c) the 20 GHz signal phase noise is further lower and the phase noise ratio is larger than 9.5 dB for all frequencies. This shows that the SHIL-QVCO has a certain phase-noise floor, which appears visible when the injected signal has a very low phase noise (Fig. 5.42c).

Phase-noise summaries have been computed for each of the three cases of Fig. 5.42. In each summary the main noise contributors are pointed out, together with the noise contribution of the 20 GHz signal. More specifically:

- Fig. 5.43 shows the noise summary of the simulation in Fig. 5.42a (i.e. 20 GHz signal phase noise of −111 dBc/Hz);
- Fig. 5.44 shows the noise summary of the simulation in Fig. 5.42b (i.e. 20 GHz signal phase noise of −131 dBc/Hz);
- Fig. 5.45 shows the noise summary of the simulation in Fig. 5.42c (i.e. 20 GHz signal phase noise of −166 dBc/Hz).

All the three noise summaries (Figs. 5.43, 5.44 and 5.45) show that, independently from the noise of the 20 GHz signal (contributions \(SH-I\) and \(SH-Q\)), a noise floor is present. In the range from 10 kHz to 100 MHz, two kinds of contributors can be distinguished: bias contributors and active-core contributors.

The bias contributors appear at offset frequencies lower than 1 MHz and are mostly characterized by a slope of −10 dB/dec. Referring to Fig. 5.37, the most important bias contributors are the bias circuits (current digital-to-analog converters (DACs) and current mirrors) of nodes \(V_{bias}\) and \(V_{gate,cps}\) of VCO-I, the bias circuits of node \(V_{gate,cps}\) of VCO-Q and the bandgap.

The active-core contributors appear at offset frequencies higher than 1 MHz and are characterized by a slope of 0 dB/dec. The most important active-core contributors are the cross-coupled transistor pair \(M_{1,2}\) (channel-thermal noise \(id\) and gate-resistance noise \(rg\)), the injecting cascodes \(M_{7,8}\) (\(id\) noise) and the quadrature-coupling transistors \(M_{3,4}\) (\(id\) noise).

The free-running SHIL-QVCO phase noise and the injection-locked SHIL-QVCO phase-noise floor, although they are different in order of magnitude, share most contributors, as visible by comparing Fig. 5.41 with Figs. 5.43, 5.44 and 5.45. With respect to

\textsuperscript{17}The 20 GHz signal is generated with an ideal voltage source \(vsource\), which is available in Cadence® library analogLib. In a \(vsource\) component, a noise power spectral density can be defined by a sequence of Noise/Frequency points with noise unit \(V^2/Hz\).
the injection-locked condition, the noise contributors in free running produce a higher noise power with a steeper slope in frequency (−30 dB/dec for the bias contributors and −20 dB/dec for the active-core contributors). This shows that, although many noise contributors are in common, the free-running SHIL-QVCO phase noise and the injection-locked SHIL-QVCO phase-noise floor are shaped by different mechanisms.
5.5 Second realization: a 55-63 GHz SHIL-QVCO with different injected frequencies in 40 nm CMOS

Figure 5.42: Simulated phase noise of SHIL-QVCO$^W_2$ locked to a sinusoidal input of 20.3 GHz with noise floor of: (a) $-111$ dBc/Hz, (b) $-131$ dBc/Hz, (c) $-166$ dBc/Hz. The SHIL-QVCO noise floor appears evident as the input noise floor is very low.
Figure 5.43: Phase-noise summary of the simulation in Fig. 5.42a.
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Figure 5.44: Phase-noise summary of the simulation in Fig. 5.42b.
Figure 5.45: Phase-noise summary of the simulation in Fig. 5.42c.
Another important contribution to the injection-locked SHIL-QVCO phase noise floor is the noise floor of the injecting circuits. The phase noise of SHIL-QVCO\(_W_2\) has been simulated in presence of the subharmonic injecting chain. The test bench is depicted in Fig. 5.46, where the SHIL-QVCO is the one depicted in Fig. 5.37 and the injecting chain is the one depicted in Fig. 5.35.

![Diagram of the test bench for the phase-noise simulation of SHIL-QVCO\(_W_2\) in presence of the subharmonic injecting chain. The SHIL-QVCO is the one depicted in Fig. 5.37 and the injecting chain is the one depicted in Fig. 5.35.](image)

The noise floor of the subharmonic injecting chain plays an important role, as shown in the simulation result of Fig. 5.47. The external 20 GHz source has a noise floor of \(-166\) dBc/Hz. Such a low noise floor is completely overwhelmed by the noise floor of the injecting chain. The SHIL-QVCO phase noise shape follows the injecting chain’s noise floor for offset frequencies up to 20 MHz, with the expected degradation factor of \(20\log_{10}(3) \approx 9.5\) dB.

The goal of all these phase-noise simulations is only to show the existence of a phase noise floor, which can limit the SHIL-QVCO performance. Such a noise floor can be affected by the subharmonic injecting circuits and by the transistors\(^{18}\) involved in the generation of the \(n\)-th harmonic, as also suggested by [Chen08].

\(^{18}\)Including the circuits biasing such transistors, such as bandgaps, current DACs and current mirrors.
Figure 5.47: Simulated phase noise of SHIL-QVCO$_{W_2}$, injection locked to a 20 GHz signal coming from the subharmonic injecting chain. In this case, the noise floor of the subharmonic injecting chain strongly affects the SHIL-QVCO phase noise.
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5.5.4 Measurement results

The 60 GHz chip, in which SHIL-QVCO\textsubscript{W2} is integrated, has been mounted on a dedicated PCB, with all the low-frequency IO pads bonded with the PCB connections and the mm-wave IO pads left free for on-chip probing (Fig. 5.48 and Fig. 5.49). The SHIL-QVCO (together with buffers, envelope detector and bias circuitry) consumes 35 mA drawn from a 0.9 V supply.

![Image](image.png)

Figure 5.48: The 40 nm chip mounted and bonded on PCB.

The measurement setup is depicted in Fig. 5.50. An external 60/6 GHz signal is injected into the chip. The 60 GHz SHIL-QVCO signal has been measured at the 60 GHz output by a spectrum analyzer pad while the downconverted signal is detected by an oscilloscope. The most important measurement instruments are:

- 60 GHz RF spectrum analyzer (Rohde&Schwarz FSU67GHz),
- 60/6 GHz signal generator (Rohde&Schwarz SMR 40),
- 67 GHz signal generator (Agilent E 8257D),
- time-domain oscilloscope with 4 channels (TEKTRONIX TDS 3054),
- signal analyzer for phase-noise measurements (AGT 5052B),
- multimeter.
Subharmonic injection locking with wide locking range

Figure 5.49: Probing setup.

Figure 5.50: Measurement setup. The 60 GHz SHIL-QVCO signal has been measured at the 60 GHz output by a spectrum analyzer pad while the downconverted signal is detected by an oscilloscope. Part of the calibration has been done through the envelope detector.
5.5 Second realization: a 55-63 GHz SHIL-QVCO with different injected frequencies in 40 nm CMOS

Locking range

The coupled-LC tank calibration has been verified, as shown in Fig. 5.51. As mentioned in Section 5.3, this is done through the envelope detector. First, \( C_1 \) is chosen for the desired coarse value of the output frequency, then \( C_2 \) is swept. No injection is applied and therefore the SHIL-QVCO is free running. The oscillation amplitude at the coupled-LC tank primary \( (L_1C_1) \) is monitored through the envelope detector and the oscillation frequency through an external spectrum analyzer. In this experiment the envelope detector’s response has a peak at \( C_2 \) setting ‘9’. Around the same setting, as expected, the free-running oscillation frequency has a steep change. After this free-running measurement, a 20 GHz injection is applied. As expected, the value of \( C_2 \) which gives a peak in the envelope detectors response gives also the largest LR.

Notice that the measurement result in Fig. 5.51 slightly differs from the simulation result of Fig. 5.38: the envelope detector output peaks at \( C_2 \) setting ‘9’ instead of ‘11’ and the free-running frequency, with \( C_2 \) setting swept from ‘3’ to ‘15’, ranges from 59.5 GHz to 63.5 GHz instead of ranging from 59.5 GHz to 64.5 GHz. This can be due to the fact that the LC-tank \( Q \) factor and the parasitic capacitances on chip slightly differ from the models used for simulation. Such a small discrepancy is typical for mm-wave designs in CMOS.

The LR can be moved over the frequency by changing \( C_1 \). Fig. 5.52 shows a LR of more than 2 GHz over a tuning range of 55-63 GHz under an injection of 20 GHz (estimated single-ended 20 GHz swing of 450 mVpp at \( M_{g,6} \) gates).

The injection locking of SHIL-QVCO\(^W_2 \) works well for several harmonic factors \( n \), namely \( n = 3, 5, 7 \) and 9, as shown in Fig. 5.53. Thanks to the use of coupled-LC tanks, the LR is relatively large (0.8 GHz) even with \( n = 9 \). The LR decrease from \( n = 3 \) to \( n = 9 \) can be explained by the fact that the 9th harmonic generation is not so efficient as the 3rd harmonic one\(^{19} \).

The LR sensitivity towards the subharmonic injected signal amplitude has been evaluated experimentally. Such a subharmonic signal, which is injected into the SHIL-QVCO, comes from differential-pair buffers with transformer loads. These buffers receive the signal from CMOS inverters operating at rail-to-rail swing. Therefore, the subharmonic injected signal is varied by varying the gain of the differential-pair buffers (see Fig. 5.35). The current consumption of these buffers is measured as well and used to simulate the subharmonic voltage swing. Fig. 5.54 and Fig. 5.55 show the measured LR and the simulated subharmonic voltage input, respectively under a 20 GHz injection and a 12 GHz injection. With respect to 20 GHz injection, injection at 12 GHz requires a higher injection amplitude for a large LR. The shape of the sensitivity curve of Fig. 5.55 shows that the LR central frequency changes with the input swing. This is most probably due to nonlinearities: second-order nonlinearities of the input swing influence the DC bias of the system and consequently may shift the LR central frequency. This is a further argument in favor of a large LR.

\( ^{19} \)The LR decrease might be due also to the non-optimal I/Q injected phase. Due to lack of time in measure-
Figure 5.51: Measured envelope detector output and LR, with $C_1$ fixed and $C_2$ swept. The envelope detector output is taken when the SHIL-QVCO is free-running. The setting '9' of $C_2$ gives a peak in the envelope response, which corresponds to a relative minimum of the free-running oscillation amplitude and to a large LR.
5.5 Second realization: a 55-63 GHz SHIL-QVCO with different injected frequencies in 40 nm CMOS

Figure 5.52: LR moved over the frequency. The LR is larger than 2 GHz, covering the range of 55 to 63 GHz, under injection of 20 GHz (i.e. \( n=3 \)).

Figure 5.53: LR for different orders of subharmonic injection.

Figure 5.54: Sensitivity of the measured LR towards the simulated 20 GHz input voltage swing (single-ended peak-peak). An input of 600 mVpp is sufficient for a large LR.
Figure 5.55: Sensitivity of the measured LR towards the simulated 12 GHz input voltage swing (single-ended peak-peak). An input of at least 800 mVpp is needed for a large LR. The LR central frequency is influenced by the input swing, most probably because of second-order nonlinearities.
As mentioned above, for the design of SHIL-QVCO\textsubscript{W2}, it has been chosen to trade off the LR in favor of a more uniform oscillation amplitude. This amplitude has been measured through the 60 GHz output buffer. The cable losses at 60 GHz have been neither deembedded nor measured carefully, since they are not of interest in this context. However, they can be estimated to about 10 dB. The oscillation amplitude over the LR has been verified for different injections:

- Fig. 5.56 shows a case with a 20 GHz injection (i.e. \( n = 3 \));
- Fig. 5.57 shows a case with a 12 GHz injection (i.e. \( n = 5 \));
- Fig. 5.58 shows a case of injection with \( n = 9 \).

In all these cases, the oscillation amplitude stays within a 5 dB margin, which is more uniform than the oscillation amplitude of SHIL-QVCO\textsubscript{W1} (Fig. 5.27).

![Graph showing oscillation frequency and amplitude](image)

Figure 5.56: SHIL-QVCO\textsubscript{W2} oscillation frequency and amplitude, over the LR, under 20 GHz injection (i.e. \( n = 3 \)). The oscillation amplitude is taken from the 60 GHz output buffer (cable losses not deembedded).
Subharmonic injection locking with wide locking range

Figure 5.57: SHIL-QVCO\textsubscript{W2} oscillation frequency and amplitude, over the LR, under 12 GHz injection (i.e. \( n=5 \)). The oscillation amplitude is taken from the 60 GHz output buffer (cable losses not deembedded).

Figure 5.58: SHIL-QVCO\textsubscript{W2} oscillation frequency and amplitude, over the LR, under 6.9 GHz injection (i.e. \( n=9 \)). The oscillation amplitude is taken from the 60 GHz output buffer (cable losses not deembedded).
5.5 Second realization: a 55-63 GHz SHIL-QVCO with different injected frequencies in 40 nm CMOS

Phase noise

If the oscillator is locked, the phase noise of a subharmonically injection-locked oscillator is expected to follow the phase noise of the injected signal with a degradation factor of $20\log_{10}(n)$. We verify this with a case where $n = 3$ and the LR is from 58.03-60.84 GHz. Fig. 5.59 shows the measured SHIL-QVCO phase noise for three cases:

- injected frequency close to the lower edge of LR (Fig. 5.59a),
- injected frequency in the middle of LR (Fig. 5.59b),
- injected frequency close to the upper edge of LR (Fig. 5.59c).

In all three cases, the SHIL-QVCO phase noise follows the injected-signal phase noise by a factor of 9.5 dB ($20\log_{10}(3)$) up to offset frequencies inferior to 100 kHz; but the degradation factor reaches about 20 dB at higher offset frequencies. In other words, a noise floor appears, which can be due by the subharmonic injecting circuits and by the transistors involved in the generation of the $n$-th harmonic, as suggested in [Chen08] and briefly discussed in Subsection 5.5.3.

The measured phase noise is uniform over the whole LR, as shown in Fig. 5.60. For the low offset frequency of 20 kHz the SHIL-QVCO phase noise follows the 20 GHz signal phase noise with the 9.5 dB factor over the whole LR. For the higher offset frequency of 1 MHz, the SHIL-QVCO phase noise settles at the noise floor of about $-105$ dBc/Hz over the whole LR.

The same phase noise behaviour has been observed for other injected frequencies, namely 60 GHz/$n$ with $n=5, 7$ and 9. The phase noise under 12 GHz injection (i.e. $n=5$) is shown for three particular injected frequencies in Fig. 5.61 and over the whole LR in Fig. 5.62. Two other cases, respectively with $n=7$ and $n=9$, are shown in Fig. 5.63 and Fig. 5.64. In all these cases, the SHIL-QVCO phase noise follows the 60 GHz/$n$ signal phase noise with the expected $20\log_{10}(n)$ factor only for offset frequencies lower than 100 kHz. For higher offset frequencies, the SHIL-QVCO phase noise settles at a noise floor of about $-105$ dBc/Hz.

The SHIL-QVCO phase-noise floor observed in measurements, about $-105$ dBC/Hz at 1 MHz offset frequency, does not match with the value obtained from simulations, $-140$ dBc/Hz at 1 MHz offset frequency (see Fig. 5.47). This discrepancy can be due to the fact that the simulated test bench (see Fig. 5.46) accounts only for certain noise sources, excluding for instance noisy supply voltages. Moreover, according to [Chen08] the noise floor under subharmonic injection locking is mostly caused by the devices involved in the $n$-th harmonic generation, which may not be well modelled by the device models. However, both measurements and simulations show the existence of a phase-noise floor under injection locking.
Figure 5.59: Phase noise of SHIL-QVCO in lock (LR = 58.03-60.84 GHz for a 20 GHz injection). SHIL-QVCO operating at: (a) the lower edge of the LR (58.2 GHz), (b) the middle of the LR (59.4 GHz) and (c) the upper edge of the LR (60.6 GHz). The spurs are due to the DC power supplies.
5.5 Second realization: a 55-63 GHz **SHIL-QVCO**
with different injected frequencies in 40 nm CMOS

Figure 5.60: Phase noise of **SHIL-QVCO** and of the 20 GHz injected external signal, over a 58.03-60.84 GHz LR: (a) at 20 kHz offset and (b) at 1 MHz offset. The phase noise is uniform over the whole LR.
Figure 5.61: Phase noise of $\text{SHIL-QVCO}_{W_2}$ in lock ($LR = 61.37$-$62.77\,\text{GHz}$ under $12\,\text{GHz}$ injection, i.e. order of harmonic injection $n=5$). SHIL-QVCO operating at: (a) the lower edge of the LR ($61.5\,\text{GHz}$), (b) the middle of the LR ($62.0\,\text{GHz}$) and (c) the upper edge of the LR ($62.5\,\text{GHz}$).
5.5 Second realization: a 55-63 GHz **SHIL-QVCO**
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**Figure 5.62:** Phase noise of the **SHIL-QVCO** and of the 12 GHz injected external signal, over a 61.37-62.77 GHz LR: (a) at 10 kHz offset and (b) at 1 MHz offset. The phase noise is uniform over the whole LR.

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**Figure 5.63:** Phase noise of **SHIL-QVCO_{W2}** in lock (LR = 61.59-62.51 GHz under 8.9 GHz injection, i.e. order of harmonic injection $n=7$).
Figure 5.64: Phase noise of SHIL-QVCO\(_w^2\) in lock (LR = 61.62-62.42 GHz under 6.9 GHz injection, i.e. order of harmonic injection \(n=9\)).
5.5 Second realization: a 55-63 GHz SHIL-QVCO with different injected frequencies in 40 nm CMOS

I/Q phase accuracy

The I/Q output phase error of SHIL-QVCO\textsubscript{W/2} depends on the subharmonic input phase. This input phase is determined by a programmable delay line (circuit in Fig. 5.35). Fig. 5.65 shows the I/Q output phase error over the LR\textsuperscript{20}, for different delay settings. Over a LR of 3 GHz, the I/Q output phase error varies within a range of 10°. It is worth noticing that the design of [Musa11] suffers from a much larger error: its simulated I/Q phase error ranges from −50° to +60° over a much narrower LR (around 500 MHz). Such a large I/Q phase error is due to the fact that in [Musa11] the subharmonic signal is injected into only one of the two VCOs forming the SHIL-QVCO. Fig 5.66 shows the I/Q output phase error for different delay settings, averaged over the entire LR. Setting "CtrlQ=15" gives the lowest (average) I/Q error. However, the I/Q error is less than 5° for all settings. Such an error can be considered small since can be compensated by the digital baseband of the receiver. The I/Q output phase of SHIL-QVCO\textsubscript{W/2} has been measured after downconversion of the 60 GHz I/Q signal to an intermediate frequency of 150 MHz.

\begin{figure}[h]
\centering
\includegraphics[width=\textwidth]{figure5.65}
\caption{I/Q phase error of SHIL-QVCO\textsubscript{W/2} over the whole LR, for different delay settings, with a 20 GHz injection (i.e. \(n=3\)) and \(C_2/C_1\) calibrated for large LR.}
\end{figure}

\textsuperscript{20}Despite averaging, the traces are not uniform over the LR. However, a trend can be observed.
Figure 5.66: Average I/Q phase error of SHIL-QVCO\textsubscript{W2} for different delay settings. The I/Q error is small ($< 5^\circ$) over all settings.
5.6 Conclusions

Coupled-LC tanks can be used to widen the locking range (LR) of subharmonically injection-locked LC-tank oscillators, thus improving their robustness against disturbances. The LR is considerably larger than what is achievable with single-LC-tank subharmonically injection-locked oscillators that have been published. The large LR can be obtained without a significant penalty in system efficiency. The use of such coupled-LC tanks has been explained in section 5.2. The coupling factor is chosen such that the tank impedance phase is close to zero degrees over a large frequency range, thus allowing a large LR. Design guidelines have been derived from an approximate analysis.

Coupled-LC tanks ease the calibration procedure, as explained in Section 5.3. The proposed procedure is mainly based on a relative measurement of the free-running oscillation amplitude. This is simpler than state-of-the-art calibrations, which are based on frequency tracking.

The coupled-LC-tank approach has been demonstrated with two 60 GHz SHIL-QVCOs. The first one, described in Section 5.4, is realized in a 40 nm low-power digital CMOS technology and integrated in a 60 GHz transceiver [Vidojkovic12] [Mangraviti12]. The SHIL-QVCO can lock over the frequency tuning range from 52 to 66 GHz with a LR of at least 9 GHz. However, the oscillation amplitude is not usable over the whole LR. The second 60 GHz SHIL-QVCO, described in Section 5.5, is realized in a 40 nm general-purpose digital CMOS technology and integrated with a subharmonic injecting chain [Mangraviti13b]. Under a 20 GHz injection, the LR is more than 2 GHz over a 55-63 GHz frequency tuning range. The SHIL-QVCO can operate also under other subharmonic injection frequencies (\(60/n\) GHz with \(n = 5, 7, 9\)), still achieving a LR larger than 0.8 GHz. The oscillation amplitude is usable over the whole LR. The calibration method proposed in section 5.3 has been experimentally validated on both SHIL-QVCOs.

The proposed SHIL-QVCO designs, together with the proposed calibration method, result into a robust 60 GHz frequency synthesis based on subharmonic injection locking.
Subharmonic injection locking with wide locking range
Chapter 6

Lock detection for subharmonically injection-locked oscillators

6.1 Introduction

Frequency synthesizers, based on subharmonic injection locking, require calibration to guarantee a robust operation. Typically, the LR of mm-wave subharmonically injection-locked oscillators is narrow (just a few hundreds of MHz). Consequently, disturbances can easily bring the system out of lock. Because of this, a runtime control is often needed. A frequency-tracking control is proposed in [Lee09]. A simplified scheme of frequency tracking is shown in Fig. 6.1a. This approach becomes complex at mm-wave frequencies because a mm-wave frequency divider is needed. Such a complexity is relaxed in [Deng12], where the mm-wave frequency divider is substituted by a mixer and a high-frequency doubler, as shown in Fig. 6.1b.

The robustness of subharmonic injection locking can be improved by making the LR so large that no runtime control is needed and only a simpler off-line calibration is sufficient [Chan08], [Mangraviti12].

This Ph.D. work proposes an off-line calibration based on lock detection. This calibration is demonstrated on a 60 GHz SHIL-QVCO and depicted in Fig. 6.1c. A lock detector (LD) mixes the 60 GHz SHIL-QVCO output signal with the subharmonic 60/n GHz. As explained in section 6.2, if the SHIL-QVCO is locked to the subharmonic signal, the LD DC output assumes a high state. If the SHIL-QVCO is unlocked, the LD DC output assumes a low state. Such a LD is realized with a simple passive mixer. Since only a DC measurement is required, the proposed calibration is simpler than frequency tracking and does not require any divider or high-frequency doubler (Fig. 6.1).
A 60 GHz SHIL-QVCO with such a lock detection has been implemented in 40 nm general-purpose CMOS technology, as described in section 6.3. A large LR (>2 GHz) is achieved by using coupled-LC tanks\textsuperscript{1}. The lock detection has been demonstrated under injection of the third subharmonic (i.e. 20 GHz) and the fifth subharmonic (i.e. 12 GHz).

A calibration algorithm, dedicated to coupled-LC-tank SHIL-QVCOs, is proposed in section 6.4. It only requires a DC measurement and involves an envelope detector and a LD, thus avoiding the need of high-frequency circuits such as frequency dividers. This makes the proposed approach simpler than the state-of-the-art approaches.

Figure 6.1: Different calibration methods for a mm-wave SHIL-QVCO: (a) frequency-tracking, (b) method in [Deng12], (c) proposed method.

\textsuperscript{1}\textsuperscript{This SHIL-QVCO is described in Chapter 5, section 5.5.}
6.2 Lock detection based on mixing

The basic function of a LD is to compare two periodic signals and to detect whether they run at the same frequency. For this purpose, this Ph.D. work uses a lock-in amplifier [BS12].

\[ s(t) = V_S \sin(\omega_s t + \theta_s), \quad (6.1) \]

and a quadrature reference at frequency \( \omega_r \) as:

\[ I_{ref}(t) = \sin(\omega_r t), \quad Q_{ref}(t) = \sin(\omega_r t + \pi/2), \quad (6.2) \]

after mixing we have:

\[ V_I = \frac{V_S}{2} \left[ \cos((\omega_s + \omega_r)t + \theta_s) + \cos((\omega_s - \omega_r)t + \theta_s) \right], \]
\[ V_Q = \frac{V_S}{2} \left[ \sin((\omega_s + \omega_r)t + \theta_s) + \sin((\omega_s - \omega_r)t + \theta_s) \right]. \quad (6.3) \]

The DC components of \( V_I \) and \( V_Q \), denoted as \( U_I \) and \( U_Q \) in Fig. 6.2, are different from zero only if \( \omega_s = \omega_r \), resulting in:

\[ U_I = \frac{V_S}{2} \cos(\theta_s), \]
\[ U_Q = \frac{V_S}{2} \sin(\theta_s). \quad (6.4) \]
Therefore the locked condition \((\omega_s = \omega_r)\) can be distinguished by the unlocked condition \((\omega_s \neq \omega_r)\) with:

\[
\begin{align*}
\omega_s \neq \omega_r & \Rightarrow U_I = U_Q = 0 \quad (i), \\
\omega_s = \omega_r & \Rightarrow \sqrt{U_I^2 + U_Q^2} = \frac{V_S}{2} \forall \theta_s \quad (ii).
\end{align*}
\]

(6.5)

In conclusion, the lock-in amplifier can be used as LD, whose DC output assumes either a low state (6.5.i) or a high state (6.5.ii) whether the source signal is unlocked or locked to the reference signal. Because of DC offset, condition (6.5.i) may not be zero. However, high state and low state can be still distinguished.

In the context of this thesis, the LD mixes the output signal of the 60 GHz SHIL-QVCO with the \(n\)-th harmonic of the subharmonic reference signal. The LD assumes then the high state when

\[
\omega_{osc} = n \times \omega_{SH},
\]

(6.6)

where \(\omega_{osc}\) and \(\omega_{SH}\) are respectively the signal frequencies of the SHIL-QVCO and the subharmonic reference. Since the \(n\)-th harmonic of the subharmonic signal is needed, a harmonic mixer is required for the LD. The low-pass filters of Fig. 6.2 need to filter the DC components from all the other harmonics, thus requiring a bandwidth inferior to \(\omega_{SH}\).
6.3 Realization: lock detection for a 55-63 GHz subharmonically injection-locked QVCO in 40 nm CMOS

A lock detector (LD), together with a coupled-LC 60 GHz SHIL-QVCO, has been realized and integrated in 40 nm general-purpose CMOS. This chip has already been introduced in section 5.5 in the context of coupled-LC tanks used to widen the LR of a SHIL-QVCO. The targets of this chip are:

• to demonstrate the lock detection explained in section 6.2;
• to demonstrate that the coupled SHIL-QVCO can be calibrated through DC measurements using the envelope detector and the LD.

6.3.1 System overview

The system consists mainly of four subblocks (see block diagram of Fig. 6.3):

• coupled-LC 60 GHz SHIL-QVCO,
• envelope detector,
• LD based on passive mixers,
• subharmonic circuitry operated at 60/n GHz, with n an odd integer.

Apart from the LD, this system has already been discussed in Chapter 5, Section 5.5. A chip micrograph, focused on the LD and the SHIL-QVCO, is reported in Fig. 6.4.

Contributions of this Ph.D. work

As already mentioned in Chapter 5, this Ph.D. has performed the design of the whole chip and the measurement characterization, including the:

• investigation and design of a SHIL-QVCO with the coupled-resonance approach for large LR and with an oscillation amplitude (relatively) uniform over the whole LR,
• design of an envelope detector for calibration,
• design of a LD,
• design of the subharmonic circuitry,
• design of the quadrature downconverting circuitry (to check the I/Q phase accuracy at an intermediate frequency, not mentioned in this chapter),
• finalization of the chip design,
• simulation of the subblocks and the whole system,
• measurement and characterization of the whole system.

A conference publication [Mangraviti13b] has been derived from what is discussed in this section.
Lock detection for subharmonically injection-locked oscillators

Figure 6.3: System block diagram including the LD.

Figure 6.4: Micrograph of the 40 nm, focusing on the SHIL-QVCO and the LD.
6.3 Realization: lock detection for a 55-63 GHz subharmonically injection-locked QVCO in 40 nm CMOS

6.3.2 Design of the lock detector

The LD mixes the SHIL-QVCO I/Q output, denoted as $s_I(t)$ and $s_Q(t)$ in Fig. 6.3, with the subharmonic I/Q injected signal $ref(t)$. The schematic is drawn in Fig. 6.5: two harmonic mixers and two low-frequency (DC) buffers. The two mixers provide a balanced I/Q load to the SHIL-QVCO. The LD harmonic mixers are implemented as passive mixers consisting of switched MOS resistors, as drawn in Fig. 6.6. The nonlinearity of these MOS devices is necessary for harmonic mixing $^2$.

![Schematic of the LD](image)

Figure 6.5: Schematic of the LD. It consists of two passive harmonic mixers and two low-frequency (DC) buffers. The mixers provide a balanced I/Q load to the SHIL-QVCO.

The low-frequency (DC) outputs of the mixers are combined according to their phase $^3$ (Fig. 6.5, left) and are then buffered by the low-frequency (DC) buffers (Fig. 6.5, right). For these buffers, a pseudodifferential circuit has been preferred to a differential one in

---

$^2$ Apart from such a nonlinearity, harmonic mixing is generally enabled by the square-wave shape of the large signals at the transistors' gates. On this chip, such a signal is buffered with resonant circuits and therefore the square-wave shape is lost.

$^3$ Given the 90° phase difference between signals 60 GHz $I^+$ and 60 GHz $Q^+$ and given that $I_{ref^+}$ and $Q_{ref^+}$ are expected to have a phase shift equivalent to 90° at 60 GHz as well, signal $out1 I^+$ is expected to be in phase with signal $out2 Q^+$, and so on for the other low-frequency signals.
order to enlarge the DC output voltage headroom. The DC signal is further brought to the IO buffers, drawn in Fig. 6.7. Such buffers are open-drain PMOS amplifiers. The drain is forced to ground off chip and the DC output current is measured and elaborated, as described in subsection 6.3.3.

Figure 6.6: I/Q passive harmonic mixer used in the LD, which mixes the 60 GHz SHIL-QVCO’s signal with the subharmonic 60 GHz\(\div n\) signal (\(I_{\text{ref}}\) and \(Q_{\text{ref}}\)).

Figure 6.7: IO buffer of the LD: open-drain PMOS. The output DC current is measured off chip with instruments providing an ideal short to ground.
6.3 Realization: lock detection for a 55-63 GHz subharmonically injection-locked QVCO in 40 nm CMOS

6.3.3 Measurement results

The 60 GHz chip, in which the LD (together with the SHIL-QVCO) is integrated, is presented in Chapter 5, subsection 5.5.4. An (incomplete) list of the measurement equipment consists of:

- 60 GHz RF spectrum analyzer (Rohde&Schwarz FSU67GHz),
- 60/n GHz signal generator (Rohde&Schwarz SMR 40),
- multimeter (monitoring the envelope detector’s output),
- DC source and meter (monitoring the LD’s output).

The measurement setup is depicted in Fig. 6.8. An external 60/n GHz signal is injected into the chip. The SHIL-QVCO has been measured through the 60 GHz output buffer. The envelope detector is monitored by a multimeter. The LD’s output currents (coming from the open-drain buffers of Fig. 6.7) are monitored by a DC meter and postprocessed as:

$$\text{out}_{LD} = \sqrt{I_{LD}^2 + Q_{LD}^2},$$

with $I_{LD}$ and $Q_{LD}$ the LD’s differential output currents. According to (6.5), $\text{out}_{LD}$ is either high or low whether the SHIL-QVCO is either locked or not.

![Measurement setup diagram](image)

Figure 6.8: Measurement setup for lock detection. The LD’s output currents (coming from open-drain buffers) are monitored by a DC meter and further postprocessed for lock detection.

Such a lock detection has been experimentally verified, as shown in Fig. 6.9, Fig. 6.10 and Fig. 6.11. Fig. 6.9 shows a case with a 20 GHz injection ($n=3$) and $C_2/C_1$ tuned for...
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large LR. The LD’s output is computed from the DC output currents $I^+, I^-, Q^+$ and $Q^-$ (shown in Fig. 6.9 over the injected frequency). According to (6.7), the LD’s output is thus $\sqrt{(I^+ - I^-)^2 + (Q^+ - Q^-)^2}$. Such an output assumes a high state when the system is locked (bottom graph of Fig. 6.9). Fig. 6.10 shows a case with $n=3$ and $C_2/C_1$ not tuned for large LR, which means narrow LR. Fig. 6.11 shows a case with a 12 GHz injection ($n=5$). In all these cases the lock condition is detected. Therefore this LD can be used also for narrow LRs and different $n$, given that the $n$-th harmonic generation is efficient in both the LD passive mixer and the SHIL-QVCO.

![Figure 6.9: SHIL-QVCO and LD outputs for a particular case of 20 GHz injection ($n=3$), where $C_2/C_1$ is tuned for large LR. The oscillation amplitude is taken from the 60 GHz output buffer (cable loss not deembedded). The LD output is computed from the LD’s output (DC) currents. The lock condition (thick line) is thus detected as high state of the LD output.](image)
Figure 6.10: SHIL-QVCO and LD outputs for a particular case of 20 GHz injection \((n=3)\) and narrow LR. The lock condition is in thick line.

Figure 6.11: SHIL-QVCO and LD outputs for injection of 12 GHz \((n=5)\). The lock condition is in thick line.
6.4 DC-based calibration of coupled-LC SHIL-QVCOs

The coupled-LC-tank SHIL-QVCO can be calibrated through the envelope detector and the LD. Like in [Deng12], the subharmonic signal frequency is assumed to be known. The following calibration is proposed (flow chart in Fig. 6.12): (i) set \(C_1\); (ii) tune \(C_2\) for large LR through the envelope detector (Fig. 5.51); (iii) sweep the subharmonic signal frequency and record, through the LD, whether the SHIL-QVCO is locked or not (Figs. 6.9-6.11). Repeating these steps for each \(C_1\) setting, the LR is known over the frequency (Fig. 5.52) without a frequency measurement. Only the DC outputs of the detectors need to be processed by a digital circuity. It is worth to emphasize that, thanks to the large LR, this calibration is not required during the runtime operation of the SHIL-QVCO.

![Flow chart of the proposed calibration.](image-url)

Figure 6.12: Flow chart of the proposed calibration. At the end, for each \(C_1\) setting, \(C_2\) is calibrated and the LR is known.
6.5 Conclusions

A subharmonically injection-locked oscillator needs to be calibrated in order to be locked at a targeted frequency. If the LR is narrow, a runtime control (frequency tracking) is needed in order to maintain lock against disturbances [Lee09]. Robustness can be improved by making the LR so large that no runtime control is needed and only an off-line calibration is sufficient [Chan08], [Mangraviti12]. In [Deng12] a calibration method is proposed for mm-wave SHIL-QVCOs, which is simpler than frequency tracking, but requires dividers and high-frequency doublers.

The large LR of coupled-LC-tank SHIL-QVCOs enables the use of a calibration method which is simpler than state of the art. It is based on a lock-in amplifier [BS12] used as lock detector (LD). The SHIL-QVCO output signal is mixed with the \( n \)-th harmonic of the subharmonic signal. If the SHIL-QVCO is locked to the subharmonic signal, the LD DC output assumes a high state. If the SHIL-QVCO is unlocked, the LD DC output assumes a low state. Since the proposed lock detection requires only a DC measurement, it is simpler than frequency tracking and does not require any divider or high-frequency doubler.

The proposed LD has been realized with a passive harmonic mixer and low-frequency (DC) buffers. The LD has been integrated with a coupled-LC 60 GHz SHIL-QVCO on a 40 nm CMOS chip. Lock detection has been experimentally verified with different injected frequencies (60/\( n \) GHz, \( n = 3, 5 \)) and for large and narrow LRs.

Finally, a calibration method has been proposed for coupled-LC SHIL-QVCOs. It involves the envelope detector described in Chapter 5 and the LD. This calibration requires only DC measurements and thus allows to characterize the LR over the whole frequency range without any frequency measurement. The large LR and the large tunability of coupled-LC-tank SHIL-QVCOs, together with this simple calibration method, offer a simple and robust approach for mm-wave frequency synthesis based on subharmonic injection locking.
Chapter 7

Conclusions and outlook

7.1 General conclusions

In this Ph.D. work some injection-locking techniques have been investigated and developed for mm-wave frequency synthesis on CMOS technology. Such techniques allow for high-frequency operations whereas traditional techniques would require larger power consumption or may even fail to work. In particular, this work has focused on frequency division and frequency multiplication. These two techniques have been introduced in Chapter 2.

Chapter 3 focuses on an inductor-less 60 GHz injection-locked frequency divider (ILFD) with modulus 4. An inductor-less implementation - an injection-locked ring oscillator - is preferred over an LC-based implementation since it is more compact and easier to design. However, the power-supply sensitivity can endanger the robustness of frequency division. This work improves robustness by adopting a hybrid load for the delay stages of the ring oscillator. The ILFD is realized in 40 nm digital low-power CMOS and is integrated in a 60 GHz phase-locked loop (PLL) operating in a receiver and a transmitter [Vidojkovic13a]. It consumes 12 mW under 1.1 V supply, achieving 2 GHz input locking range (LR).

Chapter 4 focuses on a 60 GHz local oscillator (LO) system based on subharmonic injection locking. This system is integrated in a four-path phased array receiver, realized in 90 nm CMOS. The signal coming from a lower-frequency (12 GHz) quadrature voltage-controlled oscillator (QVCO) is distributed to the four antenna paths, locking four 60 GHz subharmonically injection-locked QVCOs (SHIL-QVCOs). The 12 GHz distribution consists of CMOS inverters with inductive peaking. The 60 GHz SHIL-QVCO consumes typically 32 mW (ranging from 25 to 90 mW) under a 1.2 V supply. The typical LR is 250 MHz at 60 GHz, with a tuning range from 58 to 62 GHz. The SHIL-QVCO phase
noise follows the phase noise of the 12 GHz QVCO as expected. This LO system demonstrates the feasibility of subharmonic injection locking for mm-wave frequency synthesis and enhances the RF design modularity: all the 60 GHz circuitry is restricted into a small area on chip.

Chapter 5 focuses on a novel use of coupled-LC tanks for subharmonically injection-locked oscillators (SHILOs). Such an approach significantly enhances the LR, thus improving the system robustness. The LR is considerably larger than what is achievable with single-LC state-of-the-art implementations. This can be obtained without a significant penalty in system efficiency. This approach is implemented in two 60 GHz SHIL-QVCOs. The first SHIL-QVCO is realized in a 40 nm low-power digital CMOS technology and integrated in a 60 GHz transceiver [Mangraviti12]. The LR is more than 9 GHz and, thanks to tuning, can cover a frequency range from 52 to 66 GHz. But the oscillation amplitude is not usable over the whole LR. The second SHIL-QVCO is realized in a 40 nm general-purpose digital CMOS technology and integrated with a subharmonic injecting chain [Mangraviti13b]. Under a 20 GHz injection, the LR is more than 2 GHz over the 55-63 GHz tuning range. The SHIL-QVCO can operate also under other injection frequencies (60/n GHz with n = 5, 7, 9), still achieving a LR larger than 0.8 GHz. The oscillation amplitude is usable over the whole LR. Calibration is facilitated by an on-chip envelope detector.

Chapter 6 focuses on a lock detection mechanism, which is simpler than other state-of-the-art solutions. The key circuit is a lock-in amplifier based on harmonic mixing: the SHIL-QVCO output signal is mixed with the n-th harmonic of the subharmonic signal. If the SHIL-QVCO is locked to the subharmonic signal, the lock detector (LD) DC output assumes a high state. If the SHIL-QVCO is unlocked, the LD DC output assumes a low state. The LD, simply consisting of a passive harmonic mixer and DC buffers, is integrated with a coupled-LC 60 GHz SHIL-QVCO on a 40 nm CMOS chip. Lock detection has been experimentally verified with different injected frequencies (60/n GHz, n = 3, 5) and for large and narrow LRs. Furthermore, a calibration method is proposed for coupled-LC SHIL-QVCOs. It involves the envelope detector described in Chapter 5 and the LD. This calibration requires only DC measurements and thus allows to characterize the LR over the whole frequency range without any frequency measurement.
7.2 Key contributions

The key contributions of this Ph.D. work are here briefly summarized. The emphasis is on novelty and significance.

1. Investigation and design of an inductor-less 60-15 GHz ILFD in 40 nm CMOS (Chapter 3). It is a 15 GHz ring oscillator, with differential amplifiers as delay stages, where the 60 GHz signal is injected through the tail current sources.
   *Novelty* — The differential amplifiers use a *hybrid* load instead of the commonly used PMOS-triode load. The hybrid load consists of a differential binary-weight PMOS-triode resistive bank connected between the two differential output nodes, and two polysilicon resistors connecting the output nodes to the power-supply node.
   *Significance* — With respect to current state-of-the-art solutions, this hybrid load makes the ILFD more robust against supply disturbances, thus enhancing the robustness of the PLL.

2. Novel use of coupled-LC tanks to significantly enhance the LR of SHILOs (Chapter 5). This approach is realized and verified in two 60 GHz SHIL-QVCOs in 40 nm CMOS.
   *Novelty* — Such coupled-LC tanks exhibit an impedance whose phase is zero degrees over a large frequency range. This allows a large LR.
   *Significance* — A large LR facilitates the system calibration and makes the lock more robust against disturbances. The large LR is obtained without heavily degrading the system efficiency.

3. Simple lock detection for mm-wave SHILOs (Chapter 6). The LD is a lock-in amplifier that mixes the SHILO output signal with the subharmonic signal. The LD’s DC output assumes either a *high* or a *low* state whether the SHILO is locked or not to the subharmonic signal.
   *Novelty* — Lock is detected with a simple circuit using a DC output.
   *Significance* — This LD is simpler than other state-of-the-art solutions.

4. Simple LR calibration procedure for coupled-LC-tank SHILOs (Chapter 6). Thanks to the envelope detector and the LD, the LR of a coupled-LC-tank SHILO can be recorded for different settings. This procedure involves only DC measurements.
   *Novelty* — No frequency measurement is involved, only DC measurements are needed.
   *Significance* — Since only DC measurements are needed, this approach is simpler than current approaches based on frequency measurement.

The key contributions 2, 3 and 4 lead to a robust mm-wave frequency synthesis based on subharmonic injection locking.
7.3 Outlook

Injection-locking techniques offer to RF designers and researchers an outlook rich of opportunities, fascination and challenges. There are opportunities for mm-wave frequency synthesis in CMOS because injection locking allows for high frequency operations whereas traditional approaches would require more power or may even fail to work. The fascinating key principle of injection locking is that the unstable response of an oscillatory system is synchronized to the frequency of an external injected signal. Such a synchronization relies on nonlinearities and often challenges the robustness of the system. This Ph.D. work has investigated some of these challenges and has devised some solutions.

An inductorless 60-15 GHz ILFD has been demonstrated, where robustness is enhanced by using a hybrid load. A further work can deal with the investigation of the nonlinearities involved in the locking mechanism. Thanks to this, new designs can be made, achieving larger LRs and further enhances robustness.

A novel approach, based on coupled-LC tanks, has been demonstrated in order to significantly enhance the LR of mm-wave SHILOs. First-order design guidelines have been given. Further work can deal with:

• development of more accurate design guidelines;
• higher order of subharmonic injection (e.g. injection on the 11-th, 13-th harmonics etc.);
• application of such a novel approach to systems other than mm-wave SHILOs, such as THz frequency synthesizers.

A simple mechanism of lock detection has been demonstrated, involving a lock-in amplifier. This approach, simply using a passive harmonic mixer, appears simpler than other state of the art. Further work can deal with:

• a complete implementation involving digital circuit;
• a frequency-directing detection: not only detecting whether the SHILO is locked or not, but also detecting whether the wanted frequency falls above or below the LR. Such a direction can be extrapolated from the quadrature output of the quadrature harmonic mixer¹.

7.3.1 Injection locking versus classical approaches

Designers dealing with frequency synthesis may pose the question: injection locking or a classical approach? The answer depends on the targets and the context:

• performance (power consumption, functionality, area on chip, phase noise, robustness);

¹This is the small-signal quadrature output of the mixer when the system is unlocked. Considering the lock-in amplifier of Fig. 6.2, the quadrature output $\frac{V_I}{V_Q}$ exhibits a quadrature phase of $+90^\circ$ or $-90^\circ$ whether $\omega_s$ is higher or lower than $\omega_r$. 
• research (Ph.D. studies, publications, evaluation of new applications, evaluation of high-frequency performances in a given technology);
• demanding applications (e.g. with operating frequencies close to the cutoff frequency $f_T$ of the technology);
• human resources (how many designers available, current knowledge);
• time (long-term research, short-term product development).

An example of this trade-off can be a mm-wave frequency synthesizer: a (i) mm-wave PLL versus a (ii) mm-wave SHILO locked to a lower-frequency PLL. Approach (ii) appears interesting from a research point of view and brings some architectural advantages\(^2\). Phase noise can be comparable or even lower than approach (i), depending on the quality factor of passives [Chan08] [Musa11]. On the other hand, approach (i) may be fairly-enough feasible in very advanced CMOS technology nodes and matches better with the current knowledge of most RF designers.

However, the understanding of injection locking allows RF designers to pursue the quest for higher and higher operating frequencies in CMOS technology.

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\(^2\) Advantages such as a lower-frequency LO distribution, the absence of mm-wave dividers and a better design modularity of the mm-wave circuitry. More details in Chapter 2.
Appendix A

Approximate analysis of the coupled-LC tank’s impedances

A.1 Approximate calculation of \( Z_{\text{tank}}(\omega) \) and \( Z_{21}(\omega) \) of a coupled-LC tank

![Circuit Diagram](image)

Figure A.1: Circuit used for the calculation of \( Z_{\text{tank}}(\omega) \) and \( Z_{21}(\omega) \).

Impedances \( Z_{\text{tank}}(\omega) \) and \( Z_{21}(\omega) \) of the coupled-LC tank in Fig. A.1 are here calculated in order to locate their poles and zeros. For simplicity, we assume an infinite \( Q \) for the resonators. The position of the poles and zeros should not be significantly affected by this assumption. On the other hand, the impedance magnitudes \(|Z_{\text{tank}}(\omega)|\) and \(|Z_{21}(\omega)|\) significantly depend on \( Q \). By inspection, impedance \( Z_{\text{tank}}(\omega) \) of Fig. A.1 is found to be:

\[
Z_{\text{tank}}(\omega) \equiv Z_{11}(\omega) = \frac{1}{j\omega C_1 + Z_{-1}(\omega)}, \tag{A.1}
\]

with

\[
Z_1(\omega) = j\omega L_1 + \frac{k^2\omega^2 L_1 L_2}{j\omega L_2 + \frac{1}{j\omega C_2}}. \tag{A.2}
\]
After some calculations, it is found that:

\[
Z_{tank}(\omega) = \frac{j\omega L}{1 - \left(\frac{\omega_1^2}{\omega_p^1}\right) + \left(1 - \frac{\omega_2^2}{\omega_p^2}\right)},
\]

(A.3)

with

\[
\begin{align*}
\omega_1 &:= 1/\sqrt{L_1 C_1}, \\
\omega_2 &:= 1/\sqrt{L_2 C_2}, \\
\omega_{2k} &:= \omega_2/\sqrt{1 - k^2}.
\end{align*}
\]

(A.4)

The expression (5.1) is finally found defining \(\gamma = \omega_2/\omega_1\) and assuming

\[
|1 + \gamma^4 - 2\gamma^2| << |4k^2\gamma^2|.
\]

(A.5)

Considering \(\gamma\) as in (5.4), assumption (A.5) becomes

\[
k^2 << 4/5,
\]

(A.6)

which can be considered a valid assumption since the coupling factor \(k\) is generally low \((\approx 0.2)\) in the application proposed in this paper.

Similarly to \(Z_{11}\), the transimpedance \(Z_{21}\) is found to be

\[
Z_{21}(\omega) = \frac{j\omega k\sqrt{L_1 L_2}}{(1 - \frac{\omega^2}{\omega_{p1}^2})(1 - \frac{\omega^2}{\omega_{p2}^2})}.
\]

(A.7)

As can be seen in Fig. 5.8, \(Z_{11}(\omega)\) exhibits two peaks because of the position of the complex-conjugate poles \(\omega_{p1}\) and \(\omega_{p2}\) and the complex-conjugate zeros \(\omega_z\), with \(\omega_{p1} < \omega_z < \omega_{p2}\). Impedance \(Z_{21}(\omega)\) exhibits only one peak because it lacks the pair of complex-conjugate zeros \(\omega_z\).
A.2 Conditions for a phase plateau at $0^\circ$

The phase of $Z_{tank}(\omega)$ can be analyzed as sum of the phase contributions of each zero and each pole from expression (5.1). For simplicity, the asymptotic approximations of such phase contributions are considered. Note that here the finite $Q$ must be considered since it strongly affects the phase response.

Let us consider a pair of complex conjugate poles at $\omega = \omega_0$:

$$B_{pcc}(\omega) = \frac{1}{1 + \frac{j\omega}{Q\omega_0} - \frac{\omega^2}{\omega_0^2}}.$$  \hspace{1cm} (A.8)

Their phase contribution on Bode diagram is approximated as in Fig. A.2, where

1. $\angle B_{pcc}(\omega) = 0$ for $\omega : \log\left(\frac{\omega}{\omega_0}\right) < -\xi$,
2. $\angle B_{pcc}(\omega)$ has a slope of $\pi Q/\text{decade}$ for $\omega : -\xi < \log\left(\frac{\omega}{\omega_0}\right) < \xi$,
3. $\angle B_{pcc}(\omega) = -\pi$ for $\omega : \log\left(\frac{\omega}{\omega_0}\right) > \xi$;

where $\xi = 1/(2Q)$ is the damping factor. The frequencies at which the asymptotic approximation of $\angle B_{pcc}(\omega)$ changes slope can be defined as

$$\omega_{0a} = \omega_0/10^\xi, \quad \omega_{0b} = 10^\xi \omega_0.$$  \hspace{1cm} (A.9)

Figure A.2: Phase contribution of a pair of complex conjugate poles at $\omega = \omega_0$ (black line) and its asymptotic approximation (gray line).

If poles and zeros of (5.1) are opportuneely positioned in frequency, $Z_{tank}(\omega)$ experiences a phase plateau at $0^\circ$. For this, as suggested in Fig. A.3, we need:

$$\omega_{p1b} = \omega_{p2a}, \quad \omega_{z2a} = \omega_{p1}.$$  \hspace{1cm} (A.10)
Approximate analysis of the coupled-LC tank’s impedances

Figure A.3: Phase contributions of poles and zeros to $\angle Z_{\text{tank}}(\omega)$. With respect to Fig. 5.4, here the asymptotic behavior is considered.

with $\omega_{p1b}$, $\omega_{p2a}$ and $\omega_{za}$ defined as suggested in (A.9), which means:

$$\omega_{p1b} = 10^6 \omega_{p1}, \quad \omega_{p2a} = \omega_{p2}/10^6, \quad \omega_{za} = \omega_{z}/10^6.$$  (A.11)

Here poles and zeros are assumed to have the same $Q$ and therefore the same phase slope. Combining (A.10) and (A.11) with (5.2) we obtain (5.3) and (5.4). Notice that all these derivations are approximate since they come from an asymptotic approximation. However, they can be considered as a starting point for the circuit design.
List of publications

Conference proceedings


**Patent applications**

Bibliography


